

Use	Connections	Name	Description	Export	Clock	Base	End	IRQ	Tags	Opc...	
<input checked="" type="checkbox"/>		<div>clk_0</div>	Clock Source								
		clk_in	Clock Input		clk	exported					
		clk_in_reset	Reset Input		reset						
		clk	Clock Output		Double-click	clk_0					
		clk_reset	Reset Output		Double-click						
<input checked="" type="checkbox"/>		<div> hps_0</div>	Arria V/Cyclone V Hard Proce...								
		h2f_user1_clock	Clock Output		Double-click	hps_0_h2f_user1_cl...					
		memory	Conduit		hps_ddr3						
		hps_io	Conduit		hps						
		h2f_reset	Reset Output		Double-click						
	h2f_axi_clock	Clock Input		Double-click	clk_0						
	h2f_axi_master	AXI Master		Double-click	[h2f_axi_clock]						
	f2h_axi_clock	Clock Input		Double-click	clk_0						
	f2h_axi_slave	AXISlave		Double-click	[f2h_axi_clock]						
	h2f_lw_axi_clock	Clock Input		Double-click	clk_0						
	h2f_lw_axi_master	AXI Master		Double-click	[h2f_lw_axi_clock]						
<input checked="" type="checkbox"/>	<div>vga_clk_pll</div>	PLL Intel FPGA IP									
	refclk	Clock Input		Double-click	clk_0						
	reset	Reset Input		Double-click							
	outclk0	Clock Output		Double-click	vga_clk_pll_outclk0						
<input checked="" type="checkbox"/>	<div>vga_tiles</div>	vga_tiles									
	clock	Clock Input		Double-click	clk_0						
	reset	Reset Input		Double-click	[clock]						
	VGA	Conduit		vga	[vga_clock]						
	avalon	Avalon Memory Mapped Slave		Double-click	[clock]						
	vga_clock	Clock Input		Double-click	vga_clk_pll_outclk0						
	vga_reset	Reset Input		Double-click	[vga_clock]						