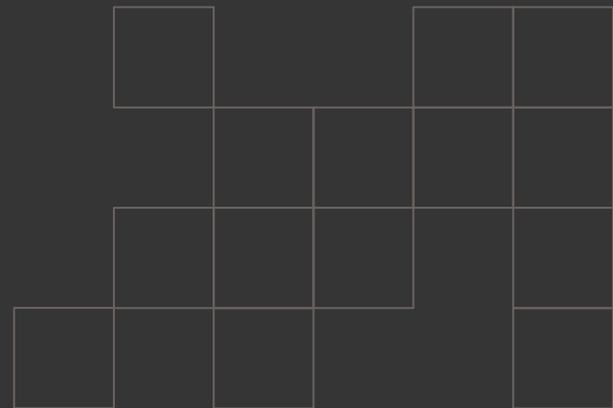


# 4840 Systolic Array Based on FPGA

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# Block Diagram

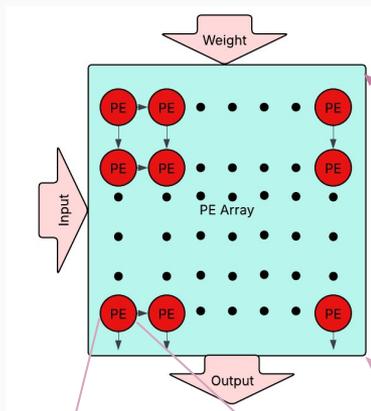


Figure 1: PE Array

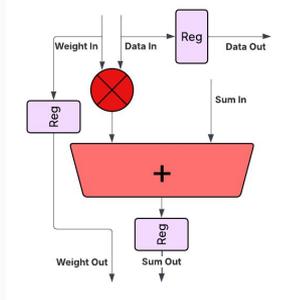


Figure 2: PE Unit

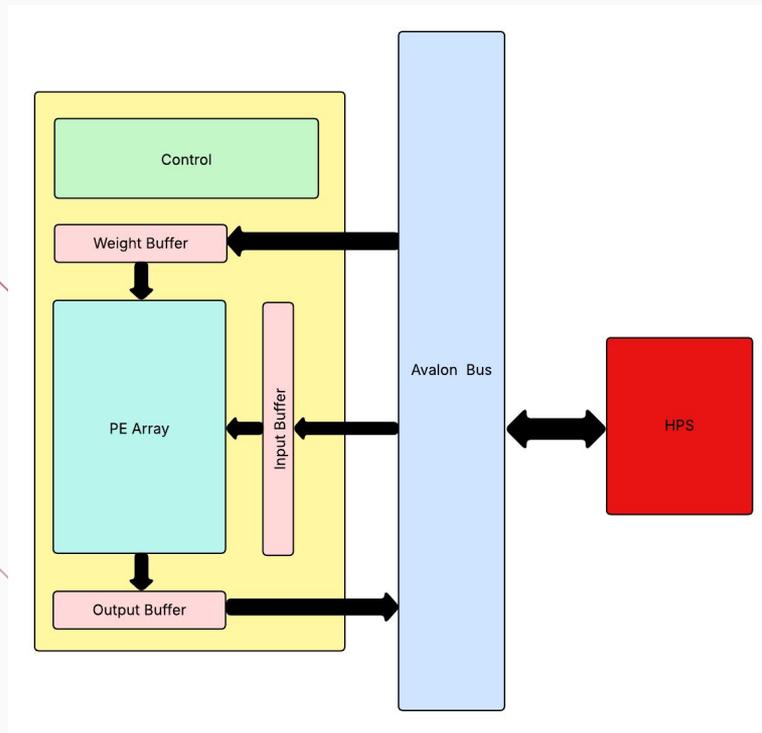


Figure 3: Block Diagram

## Control FSM & Data Flow

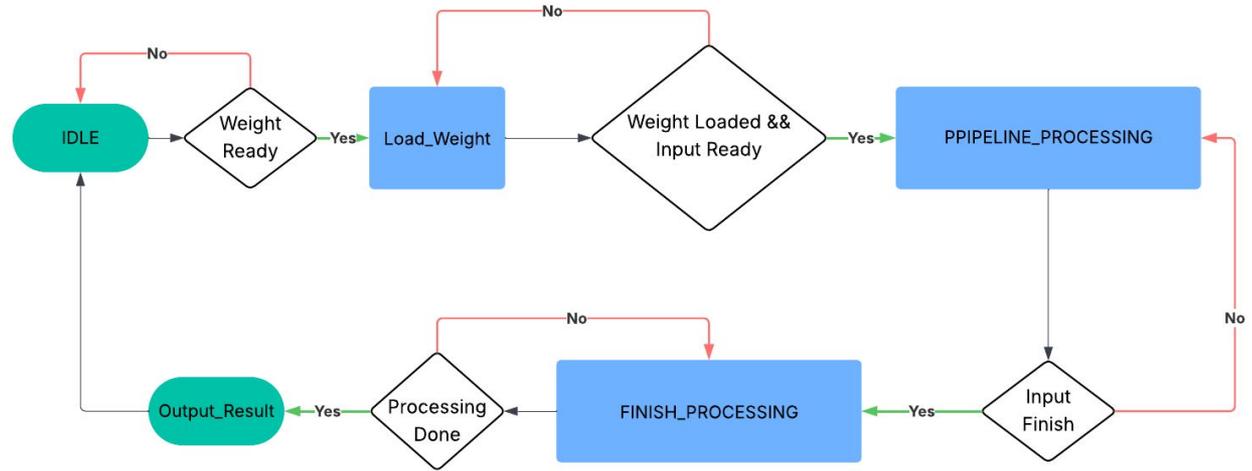
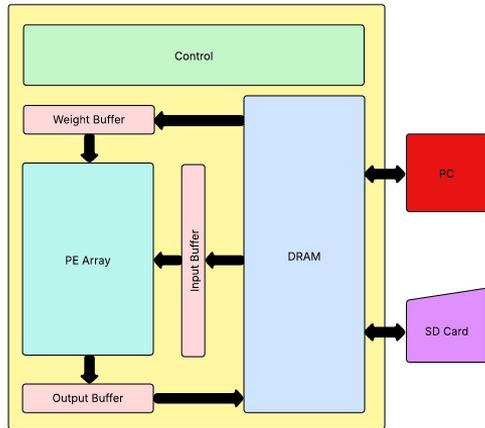


Figure 4 : FSM Diagram

# Data Flow

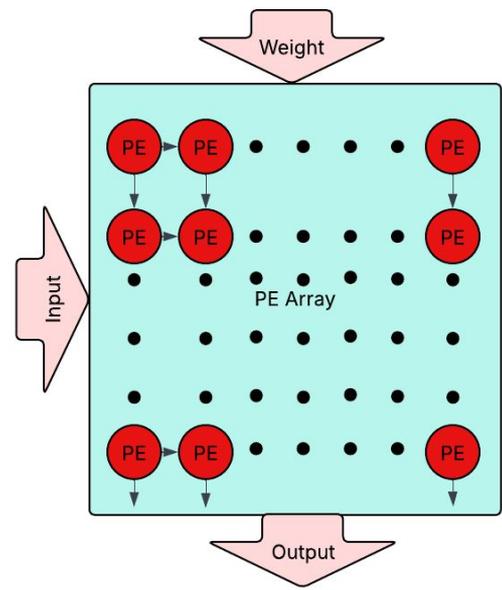
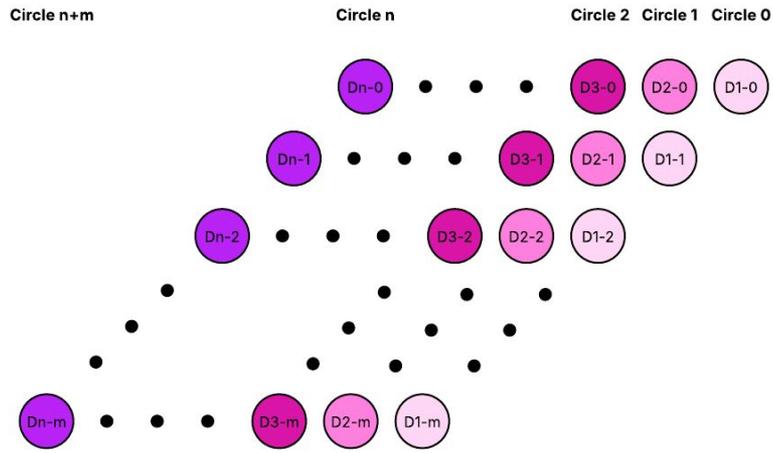
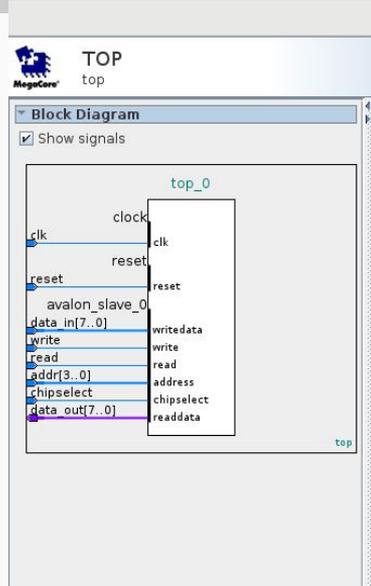


Figure 5 : Data Timing Diagram

# Synthesize

portname	Avalon Bus interface
addr	address
data_in	writedata 0 : imgsize 1 : weight_data 2 : input_data
data_out	readdata 3 : done 4 : output_data
write	write
read	read
clk	clock
reset	reset
chipselect	chipselect



The screenshot shows the Quartus Prime Lite Edition interface. The 'Analysis & Synthesis Resource Usage Summary' table is visible, showing resource utilization for the design.

Resource	Usage
Estimate of Logic Utilization (ALMs needed)	14342
Combinational ALUT usage for logic	9580
Input functions	4
Output functions	7344
Input functions	1681
Output functions	162
Input functions	389
Output functions	19651
LUT pins	25
Total MLAB memory bits	0
Total Block memory bits	1640
Total DSP Blocks	9
Maximum fan-out node	clk-input
Maximum fan-out	1987
Total fan-out	114658
Average fan-out	3.91

The message window at the bottom shows the following messages:

- 312146 Worst-case minimum pulse width slack is -2.174
- 312192 Design is not fully constrained for setup requirements
- 312282 Design is not fully constrained for hold requirements
- Quartus Prime Timing Analyzer was successful. 0 errors, 6 warnings.
- Running Quartus Prime EDA NetList Writer
- Command: quartus.eda --read settings:filesof1 --write settings:filesof2 -c 2
- 18226 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM\_PARALLEL\_PROCESSORS in your QSF to an appropriate value for best performance.
- 294915 Generated file 2.vc in folder "/home/user/stud/fal24/hy2891/4840/prj/4840/prj/quartus/simulation/node62/cis" for EDA simulation tool
- Quartus Prime EDA NetList Writer was successful. 0 errors, 3 warnings
- 293300 Quartus Prime Full compilation was successful. 0 errors, 35 warnings

Pictures for hardware synthesize

# Final Connection

System Contents    Address Map    Interconnect Requirements

System: soc\_system    Path: top\_0.avalon\_slave\_0

Use	Connections	Name	Description	Export	Clock	Base	End	IRQ	Tags	Opcode Name
<input checked="" type="checkbox"/>		<b>clk_0</b>	Clock Source		<i>exported</i>					
		clk_in	Clock Input	<b>clk</b>						
		clk_in_reset	Reset Input	<b>reset</b>	clk_0					
		clk	Clock Output	<i>Double-click to</i>						
		clk_reset	Reset Output	<i>Double-click to</i>						
<input checked="" type="checkbox"/>		<b>hps_0</b>	Arria V/Cyclone V Hard Proce...							
		h2f_user1_clock	Clock Output	<i>Double-click to</i>	hps_0_h2...					
		memory	Conduit	<b>hps_ddr3</b>						
		hps_io	Conduit	<b>hps</b>						
		h2f_reset	Reset Output	<i>Double-click to</i>						
		h2f_axi_clock	Clock Input	<i>Double-click to</i>						
		h2f_axi_master	AXI Master	<i>Double-click to</i>	clk_0					
		f2h_axi_clock	Clock Input	<i>Double-click to</i>	[h2f_axi_...]					
		f2h_axi_slave	AXI Slave	<i>Double-click to</i>	clk_0					
		h2f_lw_axi_clock	Clock Input	<i>Double-click to</i>	[f2h_axi_...]					
		h2f_lw_axi_master	AXI Master	<i>Double-click to</i>	clk_0					
					[h2f_lw_a...]					
<input checked="" type="checkbox"/>		<b>top_0</b>	TOP							
		clock	Clock Input	<i>Double-click to</i>	clk_0					
		reset	Reset Input	<i>Double-click to</i>	[clock]					
		avalon_slave_0	Avalon Memory Mapped Slave		[clock]	0x0000_0000	0x0000_000f			



```
[Compare] Pattern 1
- Max Abs Error      : 0
- Mean Abs Error     : 0.00
- Match (zero diff) : 100.00%

[Compare] Pattern 2
- Max Abs Error      : 0
- Mean Abs Error     : 0.00
- Match (zero diff) : 100.00%

[Compare] Pattern 3
- Max Abs Error      : 0
- Mean Abs Error     : 0.00
- Match (zero diff) : 100.00%
```

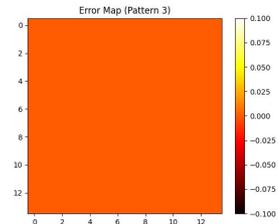
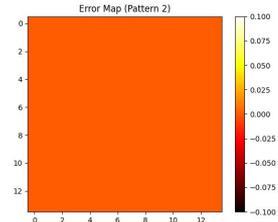
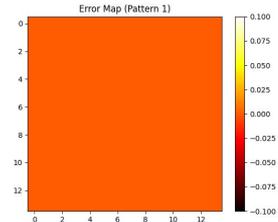


Figure 9: Verification Results

## On board test

```
if (chipselect && read && !read_prev) begin
  case (addr)
    4'h3: begin
      output_sw_en <= 0;
      data_out <= done_1;
    end
    4'h4: begin
      output_sw_en <= 1;
      data_out <= output_data;
    end
    default: begin
      data_out <= 0;
      output_sw_en <= 0;
    end
  endcase
end
else begin
  output_sw_en <= 0;
end
```

IO read is a big problem, since after we tested, the read signal will last for more than 1 cycle.  
So, we need to latch the counter even when the read is high.

```
printf("Reading output_data:\n");
for (i = 0; i < 14*14; i++) {
  output_data[i] = read_output_data();
  printf("  output_data[%d] = %d\n", i, output_data[i]);

  // Verify output_data
  if ((abs(output_data[i] * 512 - golden_data[i]) / golden_data[i]) > 0.5) {
    fprintf(stderr, "Error: output_data[%d] = %d (expected %d)\n",
            i, output_data[i], golden_data[i]);
  }
}
```

For the golden model, since the quantize scaling happens all over the computation, we need to scale back to do the comparison.