6.47. (a) \( P > D_{CQM} + D_{LM} + S + 2T_L = 2 + 16 + 3 + 2(2) = 25 \). Choose \( P = 25 \).

\( W > C_{Wm} + T_L + T_T = 2 + 2 + 3 = 7 \). Choose \( W = 12.5 \) (Half of \( P \) is advantageous.)

Then \( D_{LmB} = 2T_L + H - D_{CQM} = 2(2) - 1 - 0.5 = 2.5 \).

(b) If \( D_{LmB} \) is too large, then we must add delays in each of the FF output paths; in this case the minimum values of these delays must be 2.5-2=0.5. Then the maximum value of these delays will be 0.5(3)=1.5. This amount must be added to the period, making it 25+1.5=26.5. It would also be desirable (though not essential) to increase \( W \) to 26.5/2=13.25.

6.48. \( P > D_{DQM} + D_{LM} = 2.5 + 16 = 18.5 \), and \( P > T + D_{CQM} + D_{LM} + S + T_T - W = 2 + 2 + 16 + 3 - W = 26 - W \). The lowest possible acceptable value for \( P \) is 18.5, provided we can make \( W = 26 - 18.5 = 7.5 \). But \( W \) must satisfy the constraint: \( D_{CQM} + D_{Lm} > T_L + W + T_T + H \). This requires: \( D_{Lm} > T_L + W + T_T + H - D_{CQM} = 2 + 7.5 + 3 - 1 - 0.5 = 11 \). For case-a this is too big (maximum allowable value of \( D_{Lm} \) is 6, which is smaller by 5 units). Thus \( W \) must be decreased by 5 to 2.5. But the smallest allowable value of \( W \) is \( C_{Wm} + T_L + T_T = 2 + 2 + 3 = 7 \). Hence, we must set \( W = 7 \), which means that \( D_{Lm} \) be 6+7-2.5=10.5. Since this is too large by 10.5-6=4.5, we must add delays to the FF outputs whose minimum values make up this factor. That is, the minimum delay values must be 4.5. Then the maximum delays added will be 3(4.5)=13.5. Then, with \( D_{LM} \) thereby increased by 13.5, and with \( W = 7 \), we have \( P = 26 + 13.5 - 7 = 32.5 \).

For case-b, where \( D_{Lm} \) can be as large as 12, we can set \( W = 7.5 \) (which requires only that \( D_{Lm} \) be no more than 11) and operate with \( P = 18.5 \).

6.49. We have the constraints: \( P > D_{1DQM} + D_{2DQM} + D_{LM} \), and \( P > T_2 + D_{2CQM} + D_{LM} + S_1 + T_1 T' - V \). The first of these means that \( P > 2 + 2.5 + 16 = 20.5 \). The second means: \( P > 1.5 + 2.5 + 16 + 2.5 + 2 - V = 24.5 - V \). We can achieve the lower value if we set \( V = 24.5 - 20.5 = 4 \). But we must also satisfy the short-path constraint: \( D_{2CQM} + D_{Lm} > T_2 + V + T_1 T' + H_1 \), which, in this case translates into: \( D_{Lm} > 1.5 + 4 + 2 = 7.5 \). For case-a, this is satisfactory, and so we can set \( V = 4 \) and \( P = 20.5 \), requiring that none of the short-path delays is less than 7.5.

For case-b, we cannot ensure that the short-path delays all exceed 7.5. The best we can do is guarantee that they all exceed 4. With this value of \( D_{Lm} \), we must decrease \( V \) from 4 by the amount 7.5-4=3.5, i.e. we cannot make \( V \) larger than 4-3.5=0.5. With this value, \( P \) is determined by the second of the long-path constraints to be 24.5-0.5=24.
6.50. If the $D_1$-signal arrives early, then the delay through the $L_1$-latch is $D_{1CQM}$. In the worst case, the leading edge of $C_1$ is late by $T_{1L}$. The $C_2$-trailing edge may be early by $T_{2T}$, and the $D_2$-input must be setup $S_2$ prior to the actual trailing edge. Hence, relative to the nominal leading edge of $C_1$, the arrival time at the $D_2$-input must occur no later than $T_{1L}+D_{1CQM}+T_{2T}+S_2$. The time available for this is the distance between the nominal leading edge of $C_1$ and the nominal trailing edge of $C_2$, which, as can be seen from Fig. 6.67b, is $W_1+W_2-V$. Thus we have the constraint: $W_1+W_2-V>T_{1L}+D_{1CQM}+T_{2T}+S_2$ or: $W_1+W_2>V+T_{1L}+D_{1CQM}+T_{2T}+S_2$.

6.51. If the clock is gated, that means that there are logic devices in the path between the clock source and the C-inputs to the latches or FFs. These devices introduce additional uncertainty with respect to the arrival times of the clock-pulse edges. That is, they increase the clock-pulse edge tolerances (or skew). This has a detrimental effect on the allowable clock-pulse period. The effect is exacerbated if the logic in the various clock paths varies in complexity from one storage element to another.