1. (7 pts) Fill in the entries in the truth table below to specify the logic function described by the expression, \( Z = (A + \overline{B}C)\overline{(\overline{A} + B)} \).

Simplest approach is to multiply out and then enter ones for the resulting product terms. \( Z = AB + \overline{A} \overline{B} \overline{C} \).

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>Z</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
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<td>0</td>
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<td>0</td>
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<td>1</td>
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<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

2. (7 pts) Which, if any, of the expressions below is a minimal POS (product of sums) expression for \( A(\overline{B} + CD) + \overline{C} \)? (Show your work.)

(a) \((A + \overline{C})(\overline{B} + \overline{C} + D)\)  
(b) \(AB + ACD + \overline{C}\)  
(c) \((A + \overline{C})(\overline{B} + \overline{C})\)  
(d) \(A(\overline{B} + \overline{C})(\overline{B} + D) + \overline{C}\)  
(e) \(A(\overline{B} + \overline{C} + D)\)  
(f) none of these

Use the "adding out" technique (dual of multiplying out). \( Z = (A + \overline{C})(\overline{B} + CD + \overline{C}) = (A + \overline{C})(\overline{B} + D + \overline{C}) \)  Choice a.

3. (7 pts) Which, if any, of the logic expressions a-f describes the function realized by the circuit? (Show your work.)

(a) \(A \oplus \overline{B} \oplus C \oplus D\)  
(b) \(A \oplus B \oplus C \oplus D\)  
(c) \(\overline{A} \overline{B}(CD + C)\)  
(d) \(A \oplus B \oplus D\)  
(e) \(A \oplus C \oplus D\)  
(f) \(A \oplus D\)  
(g) None of these

ANSWER
(Enter one letter.)
Utilize the identities concerning the XOR operation. Note that complementing an XOR expression of the form $P\oplus Q\oplus \ldots \oplus R$, can be accomplished by "adding" 1 to it, OR by complementing any single item in the sum. So in this case, we can use the inverter to cancel out the inversion of the upper B-input. We then note that $X\oplus X=0$, so that the B’s and C’s cancel out. This leaves the result, $A\oplus D$ (choice f). So this is an easy problem if you approach it properly. Unfortunately, several students went back to the definition of XOR in terms of AND-OR-NOT operations and made it into a horrendous problem.

4. (7 pts) Which, if any, of the expressions a-f for $Z$ below corresponds to the following NAND-gate circuit? (Show your work.)

(a) $(A + B + C)(D + E\overline{F})$  
(b) $ABC + D(E + F)$  
(c) $ABC + D(E\overline{1} + F\overline{1})$  
(d) $(A + B + C)(D + EF)$  
(e) $ABC + (D\overline{1} + EF)$  
(f) none of these

Again, the proper approach makes all the difference. Note that the rightmost 2-stages can be transformed into an AND-to-OR circuit realizing $ABC+DQ$, where $Q$ is the output of the lower-left NAND-gate. $Q=\overline{E\overline{1}F\overline{1}}=E+F$, so the answer is $ABC+D(E+F)$ [choice b]. More generally, when faced with such a problem, the easiest approach is to transform the circuit into one involving AND-OR-INVERT elements, which is a simple matter if you utilize the two forms of NAND (or NOR).

5. (7 pts.) Using Boolean algebra theorems, determine which, if any, of the expressions a-f below is a minimal SOP (sum-of-products) expression for the function described by $Z = \overline{A}\overline{B} + \overline{C}\overline{D} + (A + B)C + \overline{D}E\overline{F}$ (Show your work.)

(a) $\overline{A}\overline{B} + \overline{C}\overline{D} + C + BC + DEF$  
(b) $\overline{A}\overline{B} + C + D$  
(c) $\overline{A}\overline{B} + \overline{C}\overline{D} + AC + BC + DEF$  
(d) $\overline{A}\overline{B} + \overline{C}\overline{D} + AC + C + D + EF$  
(e) $\overline{A} + \overline{C}\overline{D}$  
(f) none of these

One approach is to note that the first term can be written as $Q\overline{1}$, where $Q=(A+B)$. We can then use the identity, $\overline{Q}+QR=\overline{Q}+R$, to reduce the expression to $Z = \overline{A}\overline{B} + \overline{C}\overline{D} + C + DEF$.

Using the same identity again with respect to C, we get $Z = \overline{A}\overline{B} + D + C + DEF$. Using absorption ($Q+QR=Q$), we delete the last term to get
Z = \bar{A}\bar{B} + D + C [choice b]

An alternative is to multiply out to obtain Z = \bar{A}\bar{B} + \bar{C}D + AC + BC + DEF.
We can then add the consensus of \bar{A}\bar{B} and BC, which is \bar{A}C, to obtain
Z = \bar{A}\bar{B} + \bar{C}D + AC + BC + DEF + \bar{A}C. Using the uniting theorem (PQ+\bar{P}Q=Q), we reduce to
Z = \bar{A}\bar{B} + \bar{C}D + C + BC + DEF. We can now complete the solution as was done with the first approach.

6. (7 pts) Write a minimal SOP expression that describes the function realized by the circuit below?

First consider the signal at the output of the first pair of transistors. When A=1, The C-signal passes thru, so the value would be C. If A=0, the \bar{A} signal causes the left vertical NMOS transistor to pull the signal down to 0. So the signal at that point is AC. The same thing happens at the second stage, with B multiplying the logic value of the input to that stage, so the result is B(AC)=ABC.

7. (7 pts)
(a) Write the dual of the expression \( Z = A\bar{B}(C + D\bar{E}) \)
(b) Write the complement of the above expression?

For the dual, simply interchange + and multiply operations (paying careful attention to parentheses) to obtain the dual as \( A + \bar{B} + C(D + \bar{E}) \).
The complement of the original expression is easily obtained from the dual by complementing all the literals. This produces, \( \bar{A} + B + \bar{C}(\bar{D} + E) \). 

8. (7 pts) Write a logic expression corresponding directly to the transmission of the switching circuit below.

The transmission of the path thru two switches in series is the product of their transmissions, and the transmission of the path thru two switches in parallel is the sum of their transmissions.
So, for the upper path, we have \( A(BE+C) \), which then gets added to the \( D \) for the lower path to yield,

\[ A(BE+C) + D \]

9. (7 pts) On the 4-variable K-map below, map the function described by the expression

\[ Z = A(B + D) + \bar{A}(C+\bar{D}) \]

Do **NOT** do any more than simply plot the function.

![K-map diagram](image)

10. (8 pts) Suppose we are trying to find a minimal SOP expression for the function mapped below. For our *first* step, we would like to choose a subcube that is *guaranteed* (without our looking ahead) to be included in a minimal covering. Specify all the subcubes meeting this requirement, along with the point in the map that justifies this choice. State your answers in the form typified by \( ABC \), 1000. Do **not** go any further with the problem.

![K-map diagram](image)

<table>
<thead>
<tr>
<th>SUBCUBE</th>
<th>POINT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \bar{A}C )</td>
<td>0000</td>
</tr>
<tr>
<td>( \bar{B}C )</td>
<td>1010</td>
</tr>
<tr>
<td>( B\bar{C} )</td>
<td>1100</td>
</tr>
</tbody>
</table>

The points labeled q and r are each covered by only one prime implicant (pi), so choosing those pi's leads to optimal solutions, in that every optimal solution must include these
terms $B\bar{C}$ and $\bar{B}C$, respectively). The point labeled p is covered by two pi's, $\bar{A}B$ and $\bar{A}C$. But EVERY 1-point covered by $\bar{A}B$ is also covered by $\bar{A}C$, and they cost the same in terms of gate-inputs. So there is NO advantage in choosing $\bar{A}B$ instead of $\bar{A}C$ to cover p. There IS an advantage to choosing $\bar{A}C$, since it covers two 1-points not covered by $\bar{A}B$. So we can be certain that choosing $\bar{A}C$ will lead to an optimal solution. Note, in this case it turns out that there are also optimum solutions in which $\bar{A}B$ is chosen. We can designate the points by indicating the values of the variables. The requested form of the answers is as indicated in the box.

11. (8 pts) Suppose we have available as components both 2-1 and 3-1 MUX's, and that they cost the same. Use a minimum number of these components to design a 6-1 MUX. Indicate how the control signals determine which input is selected. That is, list the 6 signal inputs to the MUX along with the states of the control signals that select each input.

**ANSWERS**

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Control Signals</th>
</tr>
</thead>
<tbody>
<tr>
<td>$X_7$</td>
<td>111</td>
</tr>
<tr>
<td>$X_6$</td>
<td>110</td>
</tr>
<tr>
<td>$X_5$</td>
<td>101</td>
</tr>
<tr>
<td>$X_3$</td>
<td>011</td>
</tr>
<tr>
<td>$X_2$</td>
<td>010</td>
</tr>
<tr>
<td>$X_1$</td>
<td>001</td>
</tr>
</tbody>
</table>

12. (7 pts) Below is a partial diagram of an AND-to-OR type PLA. Add as many additional vertical lines as you need and then program the PLA to realize the three functions, $Z_1=A\bar{B}$, $Z_2=\bar{A}B$, $Z_3=A\Theta B$.

Since $A\Theta B = A\bar{B} + \bar{A}B$, we need generate only the two product terms $A\bar{B}$ and $\bar{A}B$. So we need only two of the vertical (AND-gate) lines as shown below. The $A\bar{B}$ and $\bar{A}B$ gates are each used twice.
13. (7 pts) A flow table is shown below, along with a state-assignment. Generate minimal SOP expressions for $Y_1$, $Y_2$, and $Z$.

<table>
<thead>
<tr>
<th>$X$</th>
<th>$y_1$</th>
<th>$y_2$</th>
<th>$Y_1$</th>
<th>$Y_2$</th>
<th>$Z$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>$X\bar{y}_2+Xy_1$</td>
<td>$Xy_1\bar{y}_2$</td>
<td>$Xy_1$</td>
</tr>
<tr>
<td>1</td>
<td>1,0</td>
<td>2,0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>3,0</td>
<td>1,0</td>
<td>0</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>1,0</td>
<td>3,1</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

Note that the output, $Z$ is 1 for only one position in the table. The column is specified by setting $X=1$, and the row is uniquely indicated by setting $y_1=1$. So the logic expression for $Z$ is simply $Z=Xy_1$. Since $y_1$ is 1 only in row-3, and since $Y_1$ is the NEXT value of $y_1$, we should set $Y_1$ to 1 for those table positions (total states) where the next-state (NS) entry is 3. There are two such positions. The first is specified by setting $X=0$ and $y_2=1$ (0-column, row-2), yielding the term $X\bar{y}_2$. The second location of a 3 is column-1, row-3, specified by $Xy_1$. So we have $Y_1=X\bar{y}_2+Xy_1$. Since $y_2=1$ only for row-2, we set $Y_2=1$ only for the one total state where the NS entry is 2. This is specified by $Xy_1\bar{y}_2$.

14. (7 pts) For the flow table below, find an input sequence that distinguishes states 3 and 5, i.e., an input sequence such that different output sequences result depending on whether we start in 3 or in 5. If you think there is no such sequence, justify that position.
Starting with 35, generate a chain of implications that leads to a pair with contradictory outputs for some input. Specify the input sequence leading to that pair and add the input generating the contradictory outputs. The chain that works here is: 35-(1)->26-(1)->17-(1). So the answer is 111.