# Design Languages for Embedded Systems

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## Abstract

Embedded systems are application-specific computers that interact with the physical world. Each has a diverse set of tasks to perform, and although a very flexible language might be able to handle all of them, instead a variety of problem-domain-specific languages have evolved that are easier to write, analyze, and compile.

This paper surveys some of the more important languages, introducing their central ideas quickly without going into detail. A small example of each is included.

## 1 Introduction

An embedded system is a computer masquerading as a non-computer that must perform a small set of tasks cheaply and efficiently. A typical system might have communication, signal processing, and user interface tasks to perform.

Because the tasks must solve diverse problems, a language general-purpose enough to solve them all would be difficult to write, analyze, and compile. Instead, a variety of languages have evolved, each best suited to a particular problem domain. For example, a language for signal-processing is often more convenient for a particular problem than, say, assembly, but might be poor for control-dominated behavior.

This paper describes popular hardware, software, dataflow, and hybrid languages, each of which excels a certain problems. Dataflow languages are good for signal processing, and hybrid languages combine ideas from the other three classes.

Due to space, this paper only describes the main features of each language. The author's book on the subject [10] provides many more details on all of these languages.

## 2 Hardware Languages

Verilog [14, 26] and VHDL [13, 24, 9, 2] are the most popular languages for hardware description and modeling (Figure 1). Both model systems with discrete-event semantics that ignore idle portions of the design for efficient simulation. Both describe systems with structural hierarchy: a system consists of blocks that contain instances of primitives, other blocks, or concurrent processes. Connections are listed explicitly.

Verilog provides more primitives geared specifically toward hardware simulation. VHDL's primitive are assignments such as $a = b + c$ or procedural code. Verilog adds transistor and logic gate primitives, and allows new ones to be defined with truth tables.

Both languages allow concurrent processes to be described procedurally. Such processes sleep until awakened by an event that causes them to run, read and write variables, and suspend. Processes may wait for a period of time (e.g., `#10` in Verilog,

| | Verilog | VHDL | | Verilog | VHDL |
|---|---|---|---|---|---|
| Structure | ● | ● | Type system | | ● |
| Hierarchy | ● | ● | Interface/implementation | | ● |
| Concurrency | ● | ● | Local Variables | | ● |
| Switch-level modeling | ● | ❍ | Shared memory | ● | ● |
| Gate-level modeling | ● | ❍ | Wires | ● | ● |
| Dataflow modeling | ● | ● | Resolution functions | | ● |
| Procedural modeling | ● | ● | Event access | | ● |

Table 1: Verilog and VHDL language features. ● full support ❍ partial support

```
module fulladd(ai, bi, ci, o, co);
  input ai, bi, ci;
  output o, co;
  wire s1;

  xor x1(s1, ai, bi), x2(o, s1, ci);

  assign co = (ai + bi + ci) >= 2;
endmodule

module testadd;
  reg [2:0] y;
  wire      o, co;
  reg       clk;

  fulladd a1(y[0], y[1], y[2], o, co);

  initial begin
    y = 0;  clk = 0;
    $monitor($time,,"%d%d%d %d%d",
             y[2], y[1], y[0], co, o);
  end

  always #10 clk = ~clk;
  always @(posedge clk) y <= y + 1;
endmodule
```

(a)

```
entity XOR2 is
  port (o: out Bit; a, b: in Bit);
end XOR2;

architecture arch1 of XOR2 is
begin
  A1: o <= (a xor b);
end arch1;

entity fulladd is
  port (ai, bi, ci: in Bit;
        o, co: out Bit);
end fulladd;

architecture arch1 of fulladd is
  signal s1 : Bit;
  component XOR2
    port(o: out Bit; a, b: in Bit);
  end component;
  for X1, X2: XOR2 use entity Work.XOR2;
begin
  X1: XOR2 port map (s1, ai, bi);
  X2: XOR2 port map (o, s1, ci);
  A1: co <= (ai and bi) or (ai and ci)
            or (bi and ci);
end arch1;
```

(b)

Figure 1: (a) A Verilog model for a full adder. This uses primitive gates, continuous assignment, and procedural code. (b) A similar VHDL model that does not include the test bench.

`wait for 10ns` in VHDL), a value change (`@(a or b)`, `wait on a,b`), or an event (`@(posedge clk)`, `wait on clk until clk='1'`).

VHDL communication is more disciplined and flexible. Verilog communicates through *wires* or *regs*: shared memory locations that can cause race conditions. VHDL's signals behave like wires but the resolution function may be user-defined. VHDL's variables are local to a single process unless declared shared.

Verilog's type system models hardware with four-valued bit vectors and arrays for modeling memory. VHDL does not include four-valued vectors, but its type system allows them to be added. Furthermore, composite types such as C *structs* can be defined.

Overall, Verilog is the leaner language more directly geared toward simulating digital integrated circuits. VHDL is a much larger, more verbose language capable of handing a wider class of simulation and modeling tasks.

## 3 Software Languages

Software languages describe sequences of instructions for a processor to execute. As such, most list imperative instructions executed in order that communicate through memory: an array of storage locations that hold their values until changed.

Each machine instruction typically does little more than, say, add two numbers, so high-level languages aim to specify many instructions concisely and intuitively. Arithmetic expressions are typical: coding an expression such as $ax^2 + bx + c$ in machine code is straightforward, tedious, and best done by a compiler. The C language provides such expressions, control-flow constructs such as loops and conditionals, and recursive functions. Additionally, the C++ language provides classes as a way to build new data types, templates for polymorphic code, exceptions for error handling, and a standard library of common data structures. Java is a still higher-level language that provides automatic garbage collection, threads, and monitors to synchronize them.

### 3.1 Assembly Languages

An assembly language program (Figure 2) is a list of processor instructions written in a symbolic, human-readable form. Each instruction consists of an operation such as addition along with some operands. E.g., `add r5,r2,r4` might add the contents of registers `r2` and `r4` and write the result to `r5`. Such arithmetic instructions are executed in order, but branch instructions can perform conditionals and loops by changing the processor's program counter—the address of the instruction being executed.

A processor's assembly language is defined by its opcodes, addressing modes, registers, and memories. The opcode distinguishes, say, addition from conditional branch, and an addressing mode defines how and where data is gathered and stored (e.g., from a register or from a particular memory location). Registers can be thought of as small, fast, easy-to-access pieces of memory.

### 3.2 The C Language

A C program (Figure 2b) contains functions built from arithmetic expressions structured with loops and conditionals. Instructions in a C program run sequentially, but control-flow constructs such as loops of conditionals can affect the order in which instructions execute. When control reaches a function call in an expression, control is passed to the called function, which runs until it produces a result, and control returns to continue evaluating the expression that called the function.

C derives its types from those a processor manipulates directly: signed and unsigned integers ranging from bytes to words, floating point numbers, and pointers. These can be further aggregated into arrays and structures—groups of named fields.

| | C | C++ | Java | | C++ | Java | RTOS |
|---|---|---|---|---|---|---|---|
| Expressions | ● | ● | ● | Templates | ● | | |
| Control-flow | ● | ● | ● | Namespaces | ● | ● | |
| Recursive functions | ● | ● | ● | Multiple inheritance | ● | ❍ | |
| Exceptions | ❍ | ● | ● | Threads & Locks | | ● | ● |
| Classes & Inheritance | | ● | ● | Garbage collection | ❍ | ● | |

Table 2: Software language features compared. ● full support ❍ partial support.

```
  jmp   L2          # go to L2
L1:                 # label
  movl  %ebx, %eax  # n -> m
  movl  %ecx, %ebx  # r -> n
L2:
  xorl  %edx, %edx  # clear %edx
  divl  %ebx        # m / n
  movl  %edx, %ecx  # rem -> r
  testl %ecx, %ecx  # if r = 0,
  jne   L1          # go to L1
```

(a)

```
#include <stdio.h>

int main(int argc, char *argv[])
{
  char *c;
  while (++argv, --argc > 0) {
    c = argv[0] + strlen(argv[0]);
    while (--c >= argv[0])
      putchar(*c);
    putchar('\n');
  }
  return 0;
}
```

(b)

Figure 2: (a) Euclid's algorithm in i386 assembly language. Symbols like `%ebx` represent registers. `movl` means "move long value." `divl %ebx` divides `%eax` by `%ebx` and puts the remainder in `%edx`. (b) A C program that prints its arguments backwards. The outermost while loop iterates through the arguments (count in argc, array of strings in argv), while the inner loop starts a pointer at the end of the current argument and walks it backwards, printing each character along the way. The `++` and `--` prefixes increment the variable they are attached to before returning its value.

```
class Cplx {
  double re, im;
public:
  Cplx(double v) : re(v), im(0) {}
  Cplx(double r, double i)
    : re(r), im(i) {}
  double abs() const {
    return sqrt(re*re + im*im);
  }
  void operator+= (const Cplx& a) {
    re += a.re; im += a.im;
  }
};

int main() {
  Cplx a(5), b(3,4);
  b += a;
  cout << b.abs() << '\n';
  return 0;
}
```

(a)

```
import java.io.*;
class Counter {
    int value = 0;
    boolean present = false;
    public synchronized void count() {
        try { while (present) wait(); }
        catch (InterruptedException e) {}
        value++; present = true; notifyAll();
    }
    public synchronized int read() {
        try { while (!present) wait(); }
        catch (InterruptedException e) {}
        present = false; notifyAll();
        return value;
    }
}
class Count extends Thread {
    Counter cnt;
    public Count(Counter c) { cnt = c; start(); }
    public void run() { for (;;) cnt.count(); }
}
class Mod5 {
    public static void main(String args[]) {
        Counter c = new Counter();
        Count count = new Count(c);
        int v;
        for (;;) if ( (v = c.read()) % 5 == 0 )
            System.out.println(v);
    }
}
```

(b)

Figure 3: (a) A C++ fragment illustrating a partial complex number type (the C++ standard library has a complete version). (b) A contrived Java program that spawns a counting thread to print all numbers divisible by 5.

C programs use three types of memory. Space for global data is allocated when the program is compiled, the stack stores automatic variables allocated and released when their function is called and returns, and the heap supplies arbitrarily-sized regions of memory that can be deallocated in any order.

The C language is an ISO standard, but most people consult the book by Kernighan and Ritchie [18]. Ritchie designed the language.

### 3.3 C++

C++ (Figure 3a) [25] extends C with structuring mechanisms for big programs: user-defined data types, a way to reuse code with different types, namespaces to group objects and avoid accidental name collisions when program pieces are assembled, and exceptions to handle errors. The C++ standard library includes a collection of efficient polymorphic data types such as arrays, trees, strings for which the compiler generates custom implementations.

A class defines a new data type by specifying its representation and the operations that may access and modify it. Classes may be defined by inheritance, which extends and modifies existing classes. For example, a rectangle class might add length and width fields and an area method to a shape class.

A template is a function or class that can work with multiple types. The compiler generates custom code for each different use of the template. For example, the same *min* template could be used for both integers and floating-point numbers.

### 3.4 Java

Sun's Java language [1, 16, 21] resembles C++ but is incompatible. Like C++, Java is object-oriented, providing classes and inheritance. It is a higher-level language than C++ since it uses object references, arrays, and strings instead of pointers. Java's automatic garbage collection frees the programmer from memory management.

Java provides concurrent threads (Figure 3b). Creating a thread involves extending the *Thread* class, creating instances of these objects, and calling their *start* methods to start a new thread of control that executes the objects' *run* methods.

*Synchronizing* a method or block uses a per-object lock to resolve contention when two or more threads attempt to access the same object simultaneously. A thread that attempts to gain a lock owned by another thread will block until the lock is released, which can be used to grant a thread exclusive access to a particular object.

### 3.5 RTOS

Many embedded systems use a real-time operating system (RTOS) to simulate concurrency on a single processor. An RTOS manages multiple running processes, each written in sequential language such as C. The processes perform the system's computation and the RTOS schedules them—attempts to meet deadlines by deciding which process runs when. Labrosse [19] describes the implementation of a particular RTOS.

Most RTOSes uses fixed-priority preemptive scheduling in which each process is given a particular priority (a small integer) when the system is designed. At any time, the RTOS runs the highest-priority running process, which is expected to run for a short period of time before suspending itself to wait for more data. Priorities are usually assigned using rate-monotonic analysis [7] (due to Liu and Layland [22]), which assigns higher priorities to processes that must meet more frequent deadlines.

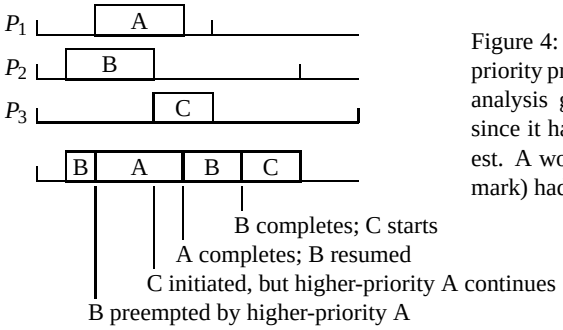


Figure 4: The behavior of an RTOS with fixed-priority preemptive scheduling. Rate-monotonic analysis gives process $P_1$ the highest priority since it has the shortest period; $P_3$ has the lowest. A would have missed its deadline (the tick mark) had it not preempted B.

## 4 Dataflow Languages

Dataflow languages describe systems of procedural processes that run concurrently and communicate through queues. Although clumsy for general applications, dataflow languages are a perfect fit for signal-processing algorithms, which use vast quantities of arithmetic derived from linear system theory to decode, compress, or filter data streams that represent periodic samples of continuously-changing values such as sound or video. Dataflow semantics are natural for expressing the block diagrams typically used to describe signal-processing algorithms, and their regularity makes dataflow implementations very efficient because otherwise costly run-time scheduling decisions can be made at compile time, even in systems containing multiple sampling rates.

### 4.1 Kahn Process Networks

Kahn Process Networks [17] form a formal basis for dataflow computation. Kahn's systems consist of processes that communicate exclusively through unbounded point-to-point first-in, first-out queues. Reading from a port makes a process wait until data is available, so the behavior of Kahn's networks does not depend on execution speeds.

Balancing processes' relative execution rates to avoid an unbounded accumulation of tokens is the challenge in scheduling a Kahn network. One general approach, proposed in Parks' thesis [23] places artificial limits on the size of each buffer. Any process that writes to a full buffer blocks until space is available, but if the system deadlocks because all buffers are full, the scheduler increases the capacity of the smallest buffer.

### 4.2 Synchronous Dataflow

Lee and Messerschmitt's Synchronous Dataflow [20] fix the communication patterns of the blocks in a Kahn network. Each time a block runs, it consumes and produces a fixed number of data tokens on each of its ports. This predictability allows SDF to be scheduled completely at compile-time, producing very efficient code.

Scheduling operates in two steps. First, the rate at which each block fires is established by considering the production and consumption rates of each block at the source and sink of each queue. For example, one of the arcs in Figure 6 implies $2C = 4D$. Once the rates are established, any algorithm that simulates the execution of the network without buffer underflow will produce a correct schedule if one exists. However, more sophisticated techniques reduce generated code and buffer sizes by better ordering the execution of the blocks (see Bhattacharyya et al. [5]).

```
process f(in int u, v; out int w)
{
  int i; bool b = true;
  for (;;) {
    i = b ? wait(u) : wait(w);
    printf("%i\n", i);
    send(i, w);
    b = !b;
  }
}

process g(in int u; out int v, w)
{
  for (;;) {
    send(wait(u), v); send(wait(u), w);
  }
}
```

```
process h(in int u, out int v, int init)
{
  send(v, init);
  for(;;)
    send(wait(u), v);
}

channel int X, Y, Z, T1, T2;
f(Y, Z, X);
g(X, T1, T2);
h(T1, Y, 0);
h(T2, Z, 1);
```

Figure 5: A Kahn Process Network [17]. The f process alternately copies from its u and v ports to its w port; the g process does the opposite, copying its u port to alternately v and w; and h simply copies its input to its output.

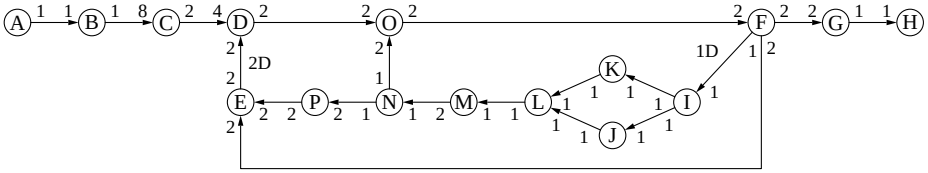


Figure 6: A modem in SDF (from Bhattacharyya et al. [6])

## 5 Hybrid Languages

Hybrid languages combine ideas from others to solve different types of problems. Esterel excels at discrete control by blending software-like control flow with the synchrony and concurrency of hardware. Polis employs extended finite-state machines communicating through single-place buffers to describe mixed hardware and software systems. Communication protocols are SDL's forte; it uses extended finite-state ma-

| | Esterel | Polis | SDL | SystemC | CCSS |
|---|---|---|---|---|---|
| Concurrent | ● | ● | ● | ● | ● |
| Hierarchy | ● | ● | ● | ● | ● |
| Preemption | ● | | | ● | ● |
| Deterministic | ● | | | ❍ | ● |
| Synchronous communication | ● | | | ● | ● |
| Buffered communication | | ● | ● | ● | ● |
| FIFO communication | | | ● | ❍ | ● |
| Procedural | ● | ❍ | ❍ | ● | ❍ |
| Finite-state machines | ● | ● | ● | ❍ | ● |
| Dataflow | | ● | ● | ● | ● |
| Multi-rate dataflow | | | | | ● |
| Software implementation | ● | ● | ● | ● | ● |
| Hardware implementation | ● | ● | | ● | ● |

Table 3: Hybrid language features compared. ● full support ❍ partial support.

```
module Example:

input  S, I;
output O;

signal R, A in
  every S do
    await I;
    weak abort
      sustain R
    when immediate A;
    emit O
  ||
    loop
      pause; pause;
      present R then emit A end;
    end
  end
end

end module
```

(a)

```
#include "systemc.h"

struct complex_mult : sc_module {
  sc_in<int>  a, b;
  sc_in<int>  c, d;
  sc_out<int> x, y;
  sc_in_clk   clock;

  void do_mult() {
    for (;;) {
      x = a * c - b * d;
      wait();
      y = a * d + b * c;
      wait();
    }
  }

  SC_CTOR(complex_mult) {
    SC_CTHREAD(do_mult, clock.pos());
  }
};
```

(b)

Figure 7: (a) An Esterel program modeling a shared resource. (b) A SystemC model for a complex multiplier.

chines with single input queues. SystemC blends styles for software and hardware in C++ to provide a smooth way to refine software models into hardware. CoCentric™ System Studio combines dataflow with Esterel-like finite-state machine semantics to simulate and synthesize dataflow applications that also require control.

### 5.1 Esterel

Intended for specifying control-dominated reactive systems, Esterel [4] combines the control constructs of an imperative software language with concurrency, preemption, and a synchronous model of time like that used in synchronous digital circuits. In each clock cycle, the program awakens, reads its inputs, produces outputs, and suspends.

An Esterel program communicates through signals that are either present or absent each cycle. In each cycle, each signal is absent unless an emit statement for the signal runs and makes the signal present for that cycle only. Esterel guarantees determinism by requiring each emitter of a signal to run before any statement that tests the signal.

### 5.2 Polis

The Polis hardware-software codesign system [3] uses a concurrent formalism geared to hardware and software implementation. A system is a collection codesign finite-state machines connected through broadcast communication channels. Each CFSM has single-place buffers for each of its inputs, and a CFSM takes a step when it receives at least one event on its inputs, whose types may be events or values. A CFSM transition is atomic, but takes an arbitrary, non-zero time. Each CFSM becomes a process running under an RTOS (buffers are in shared memory) or a state machine that takes a single clock cycle per transition.

### 5.3 SDL

SDL is a graphical specification language developed for describing telecommunication protocols defined by the ITU [15] (Ellsberger [11] is more readable). A system consists of concurrently-running FSMs, each with a single input queue, connected by channels

that define which messages they carry. Each FSM consumes the most recent message in its queue, reacts to it by changing internal state or sending messages to other FSMs, changes to its next state, and repeats the process. Each FSM is deterministic, but because messages from other FSMs may arrive in any order because of varying execution speed and communication delays, an SDL system may behave nondeterministically.

### 5.4 SystemC

The SystemC language is a C++ subset for specifying and simulating synchronous digital hardware. A SystemC specification can be simulated by compiling it with a standard C++ compiler and linking in freely-distributed class libraries (from www.systemc.org). Hardware can be generated by handing the same program to the commercially available CoCentric™ SystemC Compiler.

The SystemC language builds systems from Verilog- and VHDL-like modules. Each has a collection of I/O ports and may contain instances of other modules or processes, either synchronous or asynchronous. SystemC's simulation semantics are synchronous: when a clock arrives, each synchronous process sensitive to that clock runs, then asynchronous processes sensitive to changes on the outputs of those processes run until they stabilize, and the process repeats.

### 5.5 CoCentric System Studio

CoCentric System Studio™ [8] uses a hierarchical formalism that combines Kahn-like dataflow and hierarchical, concurrent FSMs. The FSMs resemble Harel's Statecharts [12], but use Esterel's synchronous semantics to ensure determinism.

A CCSS model is built hierarchically from Dataflow, AND, OR, and Gated models. Dataflow models are Kahn Process networks. The blocks may be dataflow primitives written in a C++ subset or other hierarchical models. AND models run concurrently and communicate with Esterel-like synchronous semantics. OR models are finite-state machines that may manipulate data and whose states may contain other models. Gated models contain sub-models whose execution can be temporarily suspended under external control.

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