Digital Instrument Multi Effects Processing Unit

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Overview

- Proposed multi-effects processor: cabinet IR, limiter effect, equalizer effect and delay effect
- Contribution: an ADC-DAC signal path, effects implementation and VGA UI
System Architecture

Digital Instrument Multi Effects processing Unit
An analog pre-amplifier is required for connecting the guitar to the DE1.
I2S Interface

WM8731 Master Mode (Left-Justified)

64x48kHz = 3.072MHz

WM8731 Master Mode (Left-Justified)

FPGA
MCLK
BCLK
LRCLK
DACDAT
ADCDAT

Figure 26 Left Justified Mode

de-serializer

128 word*16 bit FIFO (LEFT)
I2S Interface

- Avalon-ST source
  - ADC Input Data
- Avalon-ST source
  - DAC Output Data
- Exported I2S signals
- MCLK is generated separately with pll
FIR Module

Cabinet IR
- FIR Filter
- 500 configurable coeffs

Interface
- Address: 0x0000_1000 - 0x0000_13ff
- 500 FIR coefficient

\[ y[n] = \sum_{k=-\infty}^{\infty} x[k]h[n-k] \]
Clip Module

Limiter
- Clips the audio signal above a certain threshold

Interface
- Address: 0x0000_0010 - 0x0000_001f
- reg 0: threshold positive
- reg 1: threshold negative
Delay Module

Delay
- Mixing delayed sound with not delayed sound

Interface
- Address: 0x0020 - 0x0000_002f
- reg 0: Bypass
- reg 1: Delay length
- reg 2: Mix
Biquad 3-band Equalizer
Biquad 3-band Equalizer

\[ H(z) = \frac{Y(z)}{X(z)} = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{1 + a_1 z^{-1} + a_2 z^{-2}} \]

\[ y[n] = \left( \frac{b_0}{a_0} \right) x[n] + \left( \frac{b_1}{a_0} \right) x[n-1] + \left( \frac{b_2}{a_0} \right) x[n-2] - \left( \frac{a_1}{a_0} \right) y[n-1] - \left( \frac{a_2}{a_0} \right) y[n-2] \]
Biquad 3-band Equalizer

![Diagram of Biquad 3-band Equalizer]

Software
- Keyboard Input
- Slider Change
- Gain of 3 Bands
- Biquad Coefficients

Hardware
- VGA Slider Display
- Biquad Registers

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VGA User Interface

- Memory initialization file
  - background image
  - sliders and switches sprites
- Background image: 640*480, 8-bit color
- Control and select via keyboard
  - IR preset (Key 1, 2, 3, 4)
  - clip (Key Q, A)
  - delay time (Key W, S)
  - delay mix (Key E, D)
  - delay bypass (Key B, N)
  - bass (Key R, F)
  - mid (Key T, G)
  - treble (Key Y, H)
- Controller sprites position
  - preset sel, bypass sw and 6 sliders
  - stored in 8 16-bit registers
  - address: 0x0000_2000 - 0x0000_200f
## On-Chip BRAM Budget

<table>
<thead>
<tr>
<th></th>
<th>INPUT FIFO LEFT</th>
<th>INPUT FIFO RIGHT</th>
<th>FIR FIFO</th>
<th>FIR COEFF</th>
<th>VGA SPRITE</th>
</tr>
</thead>
<tbody>
<tr>
<td>SAMPLES (WORD)</td>
<td>128</td>
<td>128</td>
<td>500</td>
<td>500</td>
<td>640x480</td>
</tr>
<tr>
<td>MEMORY (BIT)</td>
<td>128x16</td>
<td>128x16</td>
<td>500x16</td>
<td>500x16</td>
<td>640x480x8</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td><strong>2478/4460Kb</strong></td>
<td></td>
<td><strong>55.6%</strong></td>
<td></td>
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</table>

## DSP BLOCK Budget

<table>
<thead>
<tr>
<th>Block Type</th>
<th>FIR</th>
<th>BIQUAD</th>
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</thead>
<tbody>
<tr>
<td>BLOCKS USED</td>
<td>2</td>
<td>20</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td>22/87</td>
<td>25.29%</td>
</tr>
</tbody>
</table>
Conclusion

● Work statement
  ○ Ziqian Deng - FIR module, delay module and clip module
  ○ Longyi Li - Top level of design and pre-amplifier hardware
  ○ Yifan Zhan - VGA user interface
  ○ Yuqi Zhu - Biquad module

● Milestone completion
  ○ Complete an ADC-DAC signal path ✓
  ○ Implement a cabinet IR ✓
  ○ Implement a boost/overdrive effect ✓
  ○ Add user interface to configure effects ✓
  ○ Add delay effect ✓

● Design files
  ○ Hardware
    ■ soc_system.sv
    ■ vga_ball.sv
    ■ i2s_avalon_st.sv
    ■ hardclip.v
    ■ delay.v
    ■ biquad.v
  ○ Software
    ■ Makefile
    ■ biquad.h/c
    ■ eq_coeff.h/c
    ■ delay.h/c
    ■ fir.h/c
    ■ hardclip.h/c
    ■ hello.c
    ■ usbkeyboard.h/c
    ■ vga_ball.h/c
Thanks for listening