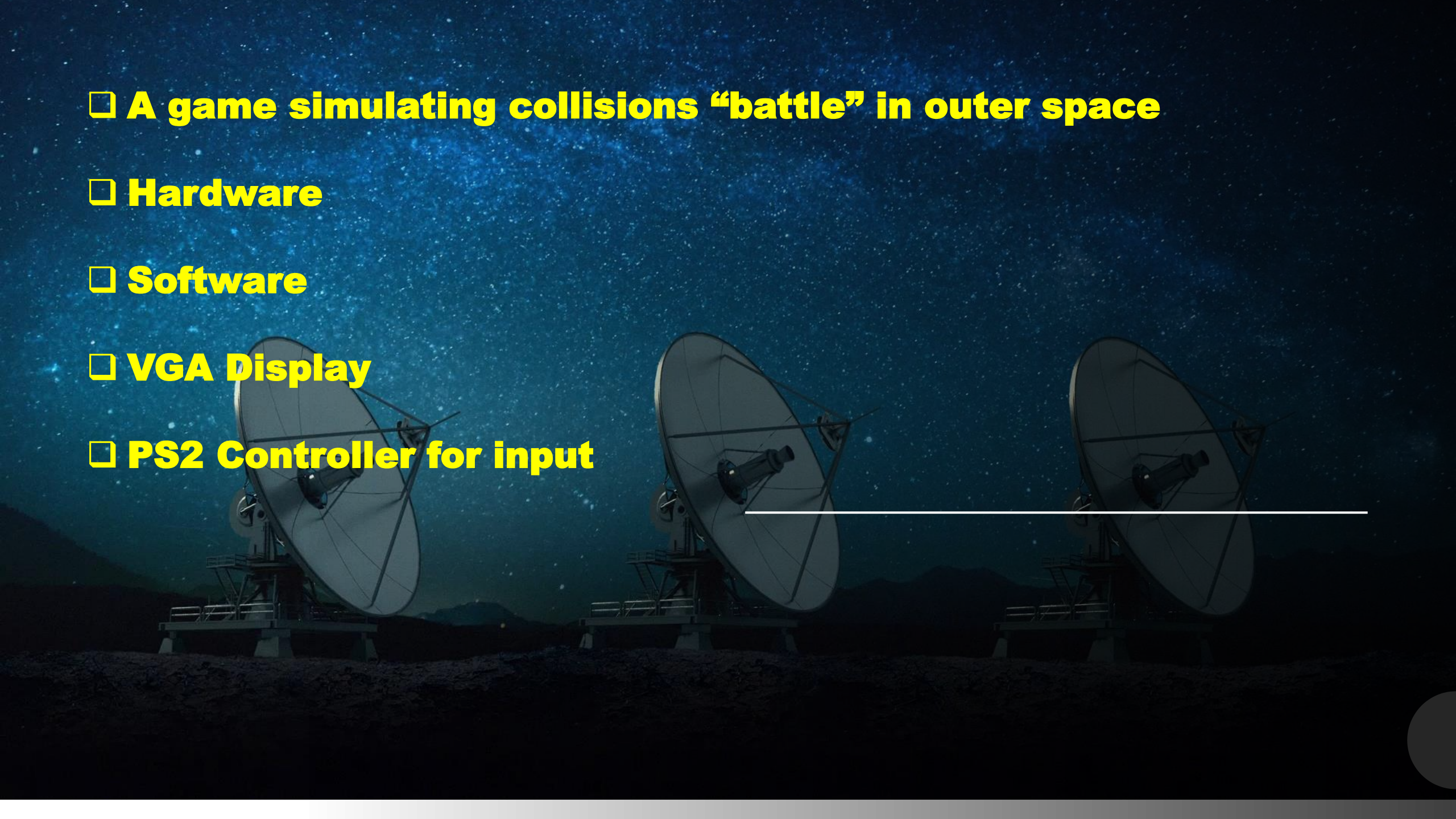
SPACE BATTLE GAME

BEN PHILIP OSURI



- A game simulating collisions “battle” in outer space
- Hardware
- Software
- VGA Display
- PS2 Controller for input

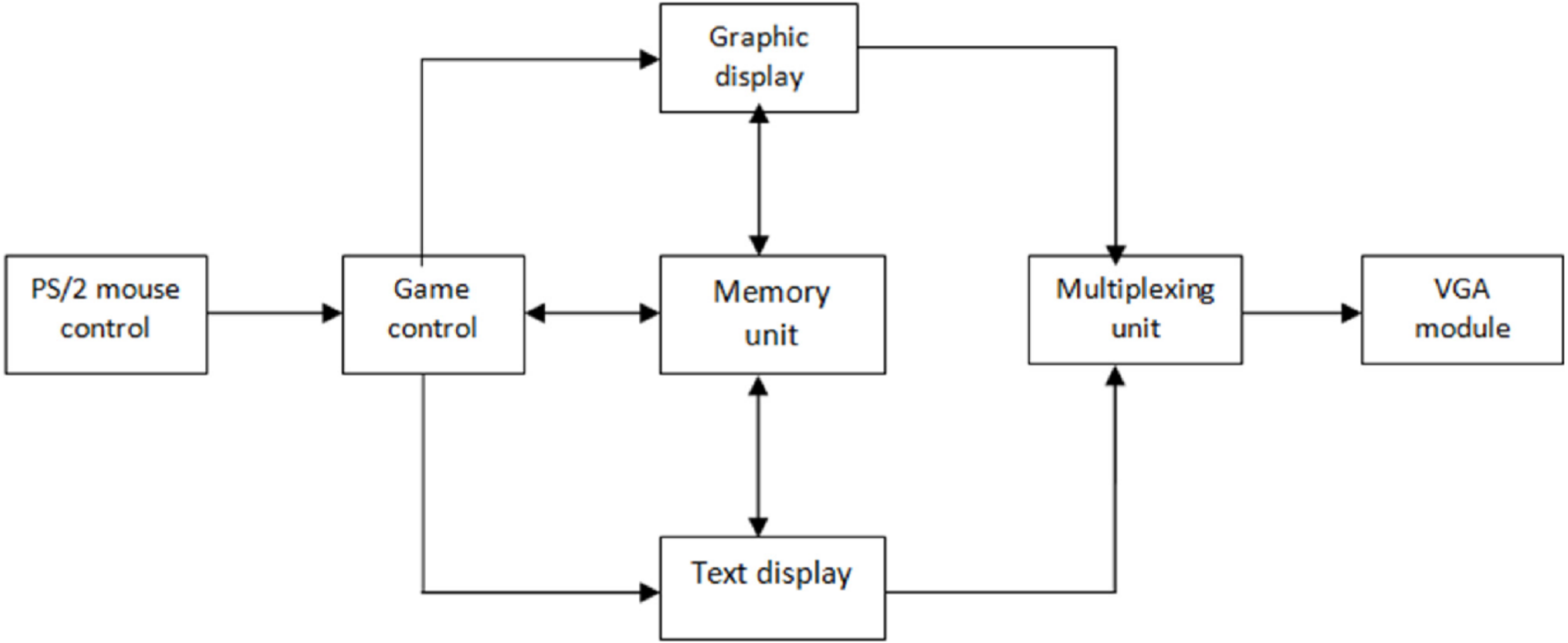
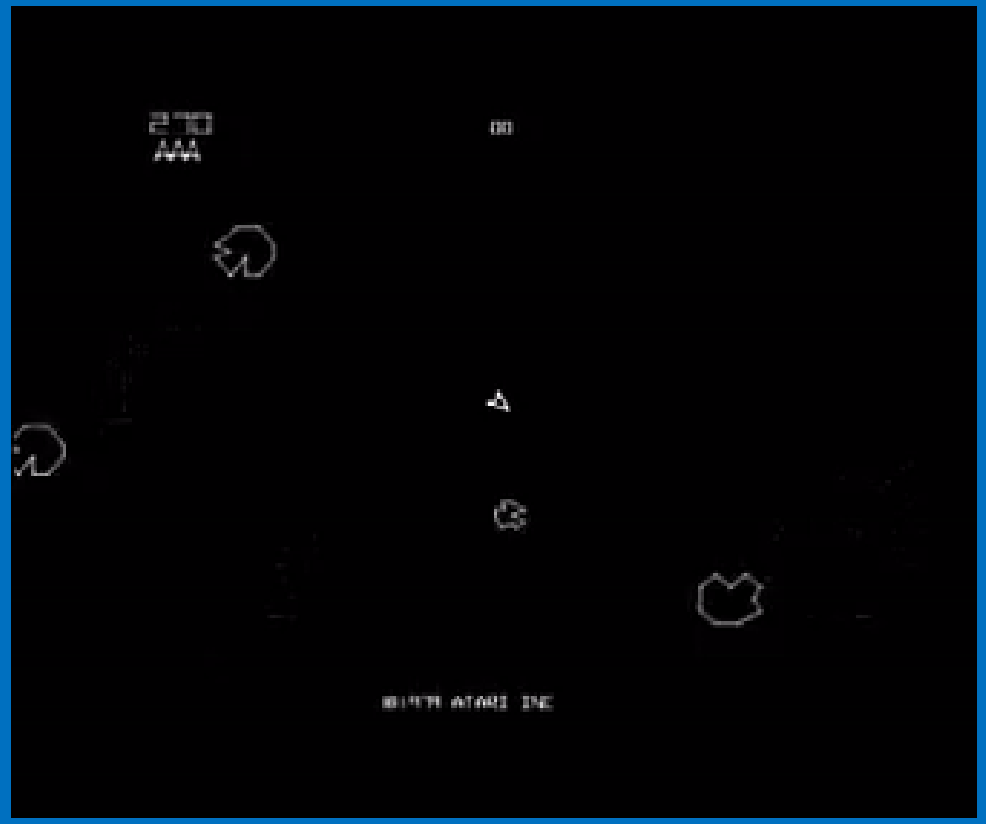


Figure 1: System Block Diagram

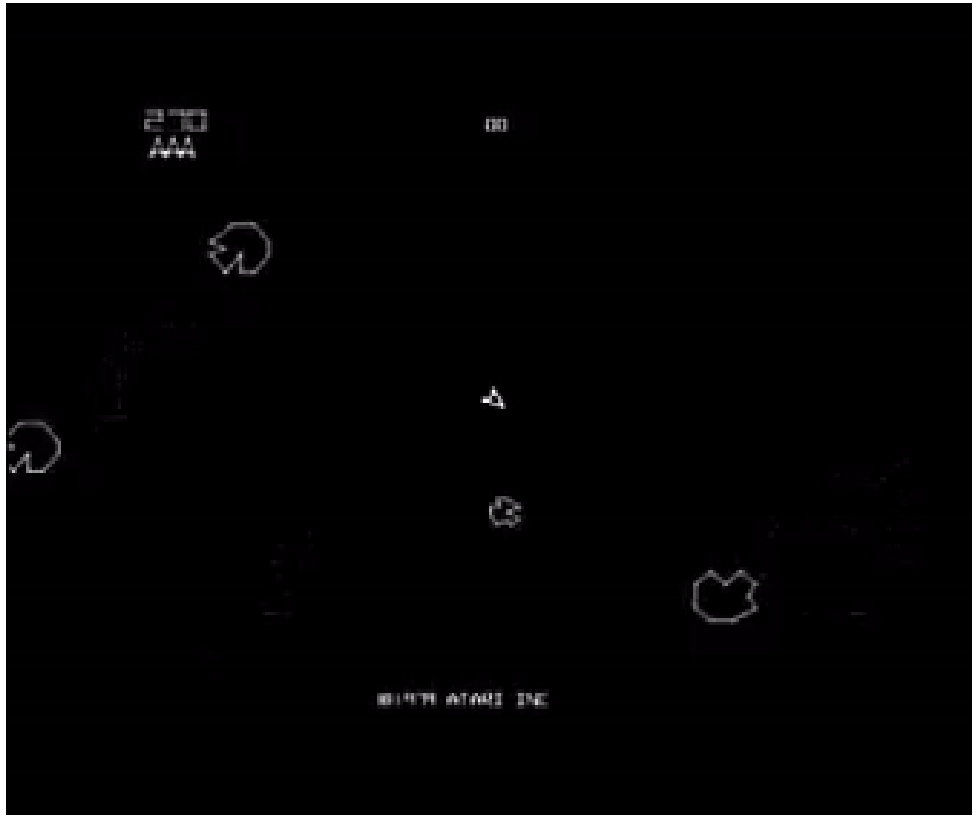
❑ HARDWARE

- ❑ Generated random numbers on the FPGA
- ❑ Used Altera Random Number Generator and Avalon FIFO memory
- ❑ Then connected FIFO memory-mapped slave to HPS through lightweight AXI master bus



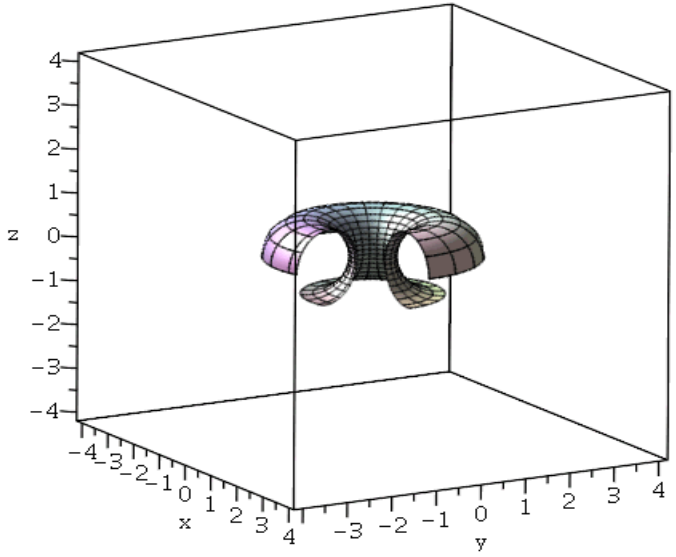
❑ SOFTWARE

- ❑ Handles much of the work like graphics and player data
- ❑ Kinematics and coordinates handled here
- ❑ Basically, game logic & what happened in each frame e.g pixel drawings and updating of objects, collision detections

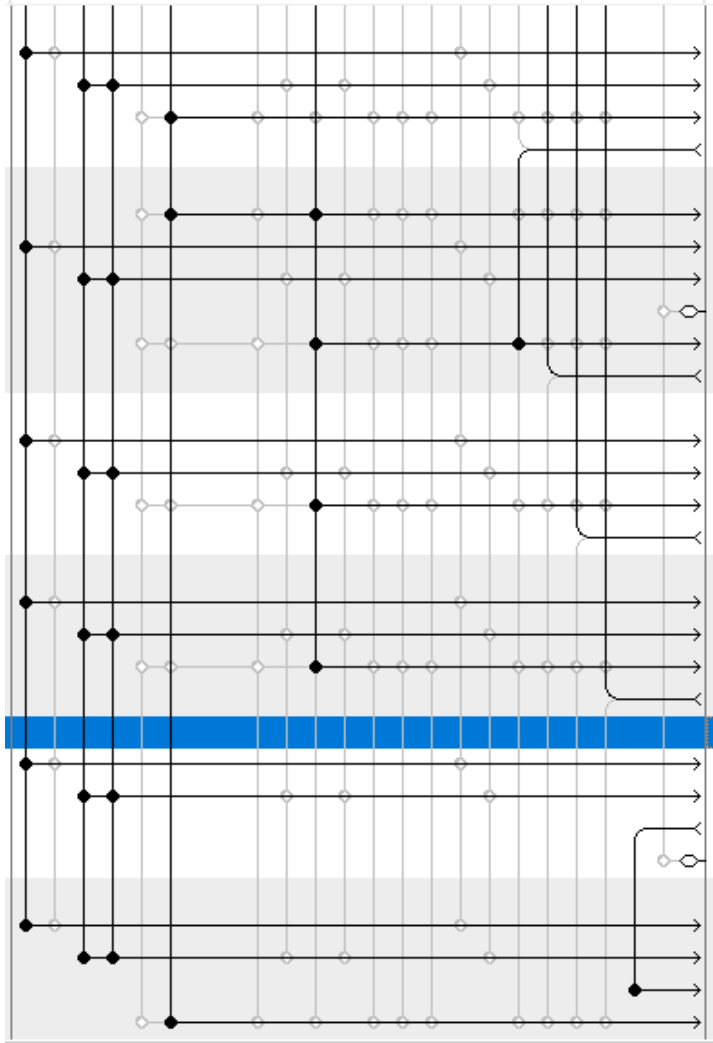


VGA: Toroidal Coordinates

- Wanted to keep objects within screen
- Usually, invisible walls around screen edges are used
- Toroidal coordinate system allowed for wrapping of objects around to the other side of screen



System: Computer_System **Path:** rand_gen_0



Name	Description	Export	Clock	Base	End
Video_In_DMA_Addr...	DMA's Front and Back Buffer Address ...				
clock	Clock Input	*Double-click to export*	**System_PLL_sys_clk**		
reset	Reset Input	*Double-click to export*	[clock]		
slave	Avalon Memory Mapped Slave	*Double-click to export*	[clock]	0x0000_3060	0x0000_306f
master	Avalon Memory Mapped Master	*Double-click to export*	[clock]		
Video_In_Subsyst...	Video_In_Subsystem				
edge_detection_contr...	Avalon Memory Mapped Slave	*Double-click to export*	[sys_clk]	mixed	mixed
sys_clk	Clock Input	*Double-click to export*	**System_PLL_sys_clk**		
sys_reset	Reset Input	*Double-click to export*			
video_in	Conduit	**video_in**			
video_in_dma_control...	Avalon Memory Mapped Slave	*Double-click to export*	[sys_clk]	mixed	mixed
video_in_dma_master	Avalon Memory Mapped Master	*Double-click to export*	[sys_clk]		
F2H_Mem_Window_...	Address Span Extender				
clock	Clock Input	*Double-click to export*	**System_PLL_sys_clk**		
reset	Reset Input	*Double-click to export*	[clock]		
windowed_slave	Avalon Memory Mapped Slave	*Double-click to export*	[clock]	0xff60_0000	0xff7f_ffff
expanded_master	Avalon Memory Mapped Master	*Double-click to export*	[clock]		
F2H_Mem_Window_...	Address Span Extender				
clock	Clock Input	*Double-click to export*	**System_PLL_sys_clk**		
reset	Reset Input	*Double-click to export*	[clock]		
windowed_slave	Avalon Memory Mapped Slave	*Double-click to export*	[clock]	0xff80_0000	0xffff_ffff
expanded_master	Avalon Memory Mapped Master	*Double-click to export*	[clock]		
rand_gen_0	Random Number Generator				
clock	Clock Input	*Double-click to export*	**System_PLL_sys_clk**		
reset	Reset Input	*Double-click to export*	[clock]		
rand_num	Avalon Streaming Source	*Double-click to export*	[clock]		
call	Conduit	**rand_gen_0_call**	[clock]		
fifo_0	Avalon FIFO Memory Intel FPGA IP				
clk_in	Clock Input	*Double-click to export*	**System_PLL_sys_clk**		
reset_in	Reset Input	*Double-click to export*	[clk_in]		
in	Avalon Streaming Sink	*Double-click to export*	[clk_in]		
out	Avalon Memory Mapped Slave	*Double-click to export*	[clk_in]	**0x0000_0010**	0x0000_0017