Spectrum of IC choices

Flexible, efficient
- Full Custom
- ASIC
- Gate Array
- FPGA
- PLD
- GP Processor
- SP Processor
- Multifunction
- Fixed-function

You choose
- Polygons (Intel)
- Circuit (Sony)
- Wires
- Logic network
- Logic function
- Program (e.g., ARM)
- Program (e.g., DSP)
- Settings (e.g., Ethernet Ctrl.)
- Part number (e.g., 74HCT00)

Cheap, quick to design
An N-Channel MOS Transistor
An N-Channel MOS Transistor

G

Oxide (SiO$_2$)

Gate

Drain (n)  Source (n)

Channel (p)
An N-Channel MOS Transistor

Gate at 0V: Off

Oxide (SiO$_2$)

Drain (n)  Source (n)

Channel (p)

Ammeter

3 V
An N-Channel MOS Transistor

Gate at 0V: Off

Oxide (SiO$_2$)

Channel (p)

Drain (n) - Source (n)

Ammeter

3 V
An N-Channel MOS Transistor

Gate at 0V: Off

Oxide (SiO$_2$)

Gate

Drain (n)

Source (n)

Channel (p)

Ammeter

3 V

0 V
An N-Channel MOS Transistor

Gate positive: On

Oxide (SiO$_2$)

Drain (n)
Source (n)

Channel (p)
CMOS Inverter Layout
CMOS Inverter Layout

![CMOS Inverter Layout Diagram]
CMOS Inverter Layout

Cross Section Through N-channel FET

Top View
The CMOS NAND Gate

Two-input NAND gate:

Two n-FETs in series; two p-FETs in parallel.
The CMOS NAND Gate

Two-input NAND gate:
- two n-FETs in series;
The CMOS NAND Gate

Two-input NAND gate:
- two n-FETs in series;
- two p-FETs in parallel
The CMOS NAND Gate

Both inputs 1:
- Both n-FETs turned on
- Output pulled low
- Both p-FETs turned off
One input 1, the other 0:
One p-FET turned on
Output pulled high
One n-FET turned on, but does not control output
The CMOS NAND Gate

Both inputs 0:
Both p-FETs turned on
Output pulled high
Full Custom: Intel 4004 Masks (2,250 Transistors)
Full Custom: Intel 4004 Die Photograph
Standard Cell ASICs
Channeled Gate Arrays
Channeled Gate Arrays
Sea-of-Gates
Gate
Arrays
FPGAs: Routing

Single-length line Switch Matrix connections

SIX PASS TRANSISTORS PER SWITCH MATRIX INTERCONNECT POINT

Double-length lines in CLB array
PLAs/CPLDs: The 22v10