Accelerated Database Processor
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Final Presentation
Motivation

- **Big Data is a new paradigm in computing**
  - we produce more data that we can possibly analyze
- **The end of dennard scaling**
  - A large portion of any chip will have to be powered off in order to stay within a power budget.
  - It makes sense to trade off area for specialized accelerators for workloads of interest
- **Accelerator for Data Mining workloads**
Introduction

- Target sql queries
- Every relation algebra operator is loosely translated into hardware (tiles)
- A database accelerator is composed of a set of tiles and an interconnect between them
Architecture Overview I
Architecture Overview II
HW/SW interface

- Fifos are memory mapped and accessed by software
  - we were hoping for DMA access
- When a stream is completed a “done” signal is propagated from the input fifos
  - this is added as an avalon st error bit
  - channel info can be used for routing
  - we need packet info in order to use altera FIFOs
Single Tile example
Testing

- verilator
- vsim
- system console
- signal tap
- on-fpga
- unit tests
- regression testing (relay station)
Lessons Learned

● Kernel programming for embedded systems is tough
● Testing testing testing ...
● bother David