Memory

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Early Memories

Williams Tube CRT-based random access memory, 1946. Used on the Manchester Mark I. 2048 bits.
Early Memories

Mercury acoustic delay line. Used in the EDASC, 1947. $32 \times 17$ bits
Early Memories

Magnetic core memory, 1952. IBM.
Early Memories

Magnetic drum memory. 1950s & 60s. Secondary storage.
<table>
<thead>
<tr>
<th>Family</th>
<th>Programmed</th>
<th>Persistence</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mask ROM</td>
<td>at fabrication</td>
<td>∞</td>
</tr>
<tr>
<td>PROM</td>
<td>once</td>
<td>∞</td>
</tr>
<tr>
<td>EPROM</td>
<td>1000s, UV</td>
<td>10 years</td>
</tr>
<tr>
<td>FLASH</td>
<td>1000s, block</td>
<td>10 years</td>
</tr>
<tr>
<td>EEPROM</td>
<td>1000s, byte</td>
<td>10 years</td>
</tr>
<tr>
<td>NVRAM</td>
<td>∞</td>
<td>5 years</td>
</tr>
<tr>
<td>SRAM</td>
<td>∞</td>
<td>while powered</td>
</tr>
<tr>
<td>DRAM</td>
<td>∞</td>
<td>64 ms</td>
</tr>
</tbody>
</table>
ROMs

3×8 decoder

enable

A₀, A₁, A₂

8×4 ROM

word 0, word 1, word 2

word line

data line

programmable connection

wired-OR

Q₃, Q₂, Q₁, Q₀

Memory – p. 7/7
EPROMs
EEPROM and FLASH

- Slow write
- Fowler-Nordheim Tunneling

EEPROM: bit at a time
FLASH: block at a time

Source: SST
Standard SRAM: 6264

Can be very fast:
Cypress sells a 55ns version
Simple, asynchronous interface

8K × 8

Address [12:0]: 10–2, 25–23, 21
Data [7:0]: 19–15, 13–11
Chip Selects: 26, 27, 22
Read Enable: 27
Write Enable: 20
Chip Select: 26
Chip Select: 22
Data Bus: D[7:0]
Address Bus: Addr[12:0]
Standard SRAM: 6264
Standard SRAM: 6264
Toshiba TC55V16256J 256K × 16

12 or 15 ns access time

Asynchronous interface

UB, LB select bytes
Toshiba TC55V16256J 256K × 16

Memory - p. 15/2
Dynamic RAM Cell

Basic problem: Leakage

Solution: Refresh
Ancient DRAM: 4164

64K × 1
Apple IIe vintage

9, 13, 10–12, 6, 7, 5
2
3
15
4

Addr[7:0]
DIN  DOUT
WE
CAS
RAS
Basic DRAM read and write cycles

RAS

CAS

Addr

WE

Din

Dout
Page mode read cycle
<table>
<thead>
<tr>
<th>Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BA[1:0]</td>
<td>Bank address</td>
</tr>
<tr>
<td>Addr[11:0]</td>
<td>Address (multiplexed)</td>
</tr>
<tr>
<td>DQ[15:0]</td>
<td>Data I/O</td>
</tr>
<tr>
<td>UDQM</td>
<td>Upper byte enable</td>
</tr>
<tr>
<td>LDQM</td>
<td>Lower byte enable</td>
</tr>
<tr>
<td>WE</td>
<td>Write enable</td>
</tr>
<tr>
<td>CAS</td>
<td>Column Address Strobe</td>
</tr>
<tr>
<td>RAS</td>
<td>Row Address Strobe</td>
</tr>
<tr>
<td>CKE</td>
<td>Clock Enable</td>
</tr>
<tr>
<td>CLK</td>
<td>Clock</td>
</tr>
</tbody>
</table>

**Synchronous interface**
- Designed for burst-mode operation
- Four separate banks; pipelined operation
Samsung 8M × 16 SDRAM

Diagram of Samsung 8M × 16 SDRAM with various components such as Bank Select, Row Buffer, Refresh Counter, Row Decoder, Column Decoder, Latency & Burst Length, Timing Register, Data Input Register, Output Buffer, I/O Control, and other control signals like RAS, CAS, WE, LRDQM, LWE, LDQM, and DQ.
### SDRAM: Control Signals

<table>
<thead>
<tr>
<th>RAS</th>
<th>CAS</th>
<th>WE</th>
<th>action</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>NOP</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Load mode register</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Active (select row)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Read (select column, start burst)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Write (select column, start burst)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Terminate Burst</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Precharge (deselect row)</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Auto Refresh</td>
</tr>
</tbody>
</table>

Mode register: selects 1/2/4/8-word bursts, CAS latency, burst on write
SDRAM: Timing with 2-word bursts

- **Clk**: Clock signal
- **RAS**: Row Address Strobe
- **CAS**: Column Address Strobe
- **WE**: Write Enable
- **Addr**: Address
- **BA**: Bank Address
- **DQ**: Data Out

The diagram illustrates the timing for different operations:
- **Load**: Load operation
- **Active**: Active operation
- **Write**: Write operation
- **Read**: Read operation
- **Refresh**: Refresh operation