Early Memories

Williams Tube CRT-based random access memory, 1946. Used on the Manchester Mark I. 2048 bits.

Early Memories

Mercury acoustic delay line. Used in the EDASC, 1947. 32 × 17 bits

Modern Memory Choices

<table>
<thead>
<tr>
<th>Family</th>
<th>Programmed</th>
<th>Persistence</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mask ROM</td>
<td>at fabrication</td>
<td>∞</td>
</tr>
<tr>
<td>PROM</td>
<td>once</td>
<td>∞</td>
</tr>
<tr>
<td>EPROM</td>
<td>1000s, UV</td>
<td>10 years</td>
</tr>
<tr>
<td>FLASH</td>
<td>1000s, block</td>
<td>10 years</td>
</tr>
<tr>
<td>EEPROM</td>
<td>1000s, byte</td>
<td>10 years</td>
</tr>
<tr>
<td>NVRAM</td>
<td>∞</td>
<td>5 years</td>
</tr>
<tr>
<td>SRAM</td>
<td>∞</td>
<td>while powered</td>
</tr>
<tr>
<td>DRAM</td>
<td>∞</td>
<td>64 ms</td>
</tr>
</tbody>
</table>

ROMs

EPROMs

EEPROM and FLASH

Slow write
Fowler-Nordheim Tunneling
EEPROM: bit at a time
FLASH: block at a time
Source: SST
Static RAM Cell

Word

Bit

Standard SRAM: 6264

19–15, 13–11
10–2, 25–23, 22

D[7:0]

Addr[12:0]

28
27
26
25
24
23
22
21

8K × 8

Can be very fast:

Cypress sells a 55ns version

Simple, asynchronous interface

Standard SRAM: 6264

Addr

Data

Toshiba TC55V16256J 256K × 16

38–35, 32–29, 16–13, 10–7

D[15:0]

Addr[17:0]

12 or 15 ns access time

Asynchronous interface

UB, LB select bytes

Ancient DRAM: 4164

64K × 1

Apple IIe vintage

Basic problem: Leakage

Solution: Refresh

Dynamic RAM Cell

Basic DRAM read and write cycles

Basic problem: Leakage

Solution: Refresh
Page mode read cycle

#### Samsung 8M × 16 SDRAM

<table>
<thead>
<tr>
<th>Bank address</th>
<th>Address (multiplexed)</th>
<th>Data I/O</th>
<th>Upper byte enable</th>
<th>Lower byte enable</th>
<th>Write enable</th>
<th>Column Address Strobe</th>
<th>Row Address Strobe</th>
<th>Clock Enable</th>
<th>Clock</th>
</tr>
</thead>
<tbody>
<tr>
<td>21, 20</td>
<td>15</td>
<td>3</td>
<td>15</td>
<td>3</td>
<td>15</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
</tr>
</tbody>
</table>

Synchronous interface

- Designed for burst-mode operation
- Four separate banks; pipelined operation

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SDRAM: Control Signals

<table>
<thead>
<tr>
<th>RAS</th>
<th>CAS</th>
<th>WE</th>
<th>action</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>NOP</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Load mode register</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Active (select row)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Read (select column, start burst)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Write (select column, start burst)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Terminate Burst</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Precharge (deselect row)</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Auto Refresh</td>
</tr>
</tbody>
</table>

Mode register: selects 1/2/4/8-word bursts, CAS latency, burst on write

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SDRAM: Timing with 2-word bursts