**Memory**

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**Early Memories**

Williams Tube CRT-based random access memory, 1946. Used on the Manchester Mark I. 2048 bits.

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**Early Memories**

Mercury acoustic delay line. Used in the EDASC, 1947. 32 × 17 bits

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**Modern Memory Choices**

<table>
<thead>
<tr>
<th>Family</th>
<th>Programmed Persistence</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mask ROM</td>
<td>at fabrication</td>
</tr>
<tr>
<td>PROM</td>
<td>once</td>
</tr>
<tr>
<td>EPROM</td>
<td>1000s, UV, 10 years</td>
</tr>
<tr>
<td>FLASH</td>
<td>1000s, block, 10 years</td>
</tr>
<tr>
<td>EEPROM</td>
<td>1000s, byte, 10 years</td>
</tr>
<tr>
<td>NVRAM</td>
<td>5 years</td>
</tr>
<tr>
<td>SRAM</td>
<td>while powered</td>
</tr>
<tr>
<td>DRAM</td>
<td>64 ms</td>
</tr>
</tbody>
</table>

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**ROMs**

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**EPROMs**

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**EEPROM and FLASH**

Slow write
Fowler-Nordheim Tunneling
EEPROM: bit at a time
FLASH: block at a time
Source: SST
Static RAM Cell

Word

Bit

19–15, 13–11
10–2, 25–23
22, 21
8K × 8
Can be very fast:
Cypress sells a 55ns version
Simple, asynchronous interface

Toshiba TC55V16256J 256K × 16

Toshiba TC55V16256J 256K × 16

Basic DRAM read and write cycles

RAS

CAS

Addr

Din

Dout

RAS

CAS

Addr

Din

Dout

Dynamic RAM Cell

Row

Column

Basic problem: Leakage
Solution: Refresh

Apple IIe vintage

64K × 1

Ancient DRAM: 4164

Basic problem: Leakage
Solution: Refresh

Apple IIe vintage

64K × 1

Basic DRAM read and write cycles

RAS

CAS

Addr

Din

Dout
Page mode read cycle

Samsung 8M × 16 SDRAM

RAS  CAS  WE  action
1   1   1   NOP
0   0   0   Load mode register
0   1   1   Active (select row)
1   0   1   Read (select column, start burst)
1   0   0   Write (select column, start burst)
1   1   0   Terminate Burst
0   1   0   Precharge (deselect row)
0   0   1   Auto Refresh

Mode register: selects 1/2/4/8-word bursts, CAS latency, burst on write

SDRAM: Control Signals

SDRAM: Timing with 2-word bursts

Bank address
Address (multiplexed)
Upper byte enable
Lower byte enable
Write enable
Column Address Strobe
Row Address Strobe
Clock Enable
Clock

Synchronous interface
Designed for burst-mode operation
Four separate banks; pipelined operation