Memory

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Williams Tube CRT-based random access memory, 1946. Used on the Manchester Mark I. 2048 bits.
Early Memories

Mercury acoustic delay line.
Used in the EDASC, 1947.
32 × 17 bits
Magnetic core memory, 1952. IBM.
Early Memories

Magnetic drum memory. 1950s & 60s. Secondary storage.
# Modern Memory Choices

<table>
<thead>
<tr>
<th>Family</th>
<th>Programmed</th>
<th>Persistence</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mask ROM</td>
<td>at fabrication</td>
<td>∞</td>
</tr>
<tr>
<td>PROM</td>
<td>once</td>
<td>∞</td>
</tr>
<tr>
<td>EPROM</td>
<td>1000s, UV</td>
<td>10 years</td>
</tr>
<tr>
<td>FLASH</td>
<td>1000s, block</td>
<td>10 years</td>
</tr>
<tr>
<td>EEPROM</td>
<td>1000s, byte</td>
<td>10 years</td>
</tr>
<tr>
<td>NVRAM</td>
<td>∞</td>
<td>5 years</td>
</tr>
<tr>
<td>SRAM</td>
<td>∞</td>
<td>while powered</td>
</tr>
<tr>
<td>DRAM</td>
<td>∞</td>
<td>64 ms</td>
</tr>
</tbody>
</table>
ROMs

8 × 4 ROM

3x8 decoder

enable

A₀
A₁
A₂

word 0
word 1
word 2

word line

data line

programmable connection

wired-OR

Q₃
Q₂
Q₁
Q₀
EPROMs
EEPROM and FLASH

- Slow write
- Fowler-Nordheim Tunneling

EEPROM: bit at a time
FLASH: block at a time

Source: SST
Static RAM Cell
Standard SRAM: 6264

8K × 8
Can be very fast:
Cypress sells a 55ns version
Simple, asynchronous interface
Standard SRAM: 6264

CS1

CS2

WE

OE

Addr

Data
Features

- 55, 70 ns access times
- CMOS for optimum speed/power
- Easy memory expansion with CE1, CE2, and OE features
- TTL-compatible inputs and outputs
- Automatic power-down when deselected

Functional Description

The CY6264 is a high-performance CMOS static RAM organized as 8192 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable (CE1), an active HIGH chip enable (CE2), and active LOW output enable (OE) and three-state drivers. Both devices have an automatic power-down feature (CE1), reducing the power consumption by over 70% when deselected. The CY6264 is packaged in a 450-mil (300-mil body) SOIC.

An active LOW write enable signal (WE) controls the writing/reading operation of the memory. When CE1 and WE inputs are both LOW and CE2 is HIGH, data on the eight data input/output pins (I/O0 through I/O7) is written into the memory location addressed by the address present on the address pins (A0 through A12). Reading the device is accomplished by selecting the device and enabling the outputs, CE1 active LOW, CE2 active HIGH, while WE remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable (WE) is HIGH. A die coat is used to insure alpha immunity.

Logic Block Diagram Pin Configuration

The image shows a detailed logic block diagram of the CY6264 static RAM, including inputs (A0-A12, CE1, CE2, WE, OE), outputs (I/O0-I/O7), and internal components like the Row Decoder, Column Decoder, Input Buffer, 256 x 32 x 8 Array, and Sense Amps. The diagram also highlights the connections and control signals that enable the memory's functionality.
Toshiba TC55V16256J 256K × 16

12 or 15 ns access time
Asynchronous interface
UB, LB select bytes
Dynamic RAM Cell

Basic problem: Leakage

Solution: Refresh
Ancient DRAM: 4164

64K × 1
Apple IIe vintage

9,13,10–12,6,7,5

Addr[7:0]
DIN   DOUT
WE
CAS
RAS

Memory – p. 17/2
Basic DRAM read and write cycles

- **RAS**
- **CAS**
- **Addr**: Row Col Row Col
- **WE**
- **Din**: Hatched area
- **Dout**: Solid line
Page mode read cycle

- **RAS**: Active low
- **CAS**: Active high
- **Addr**: Row, Col
- **WE**: Write enable
- **Din**: Data input (active high)
- **Dout**: Data output (active low)
## Samsung 8M × 16 SDRAM

### Pinouts

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BA[1:0]</td>
<td>Bank address</td>
</tr>
<tr>
<td>Addr[11:0]</td>
<td>Address (multiplexed)</td>
</tr>
<tr>
<td>DQ[15:0]</td>
<td>Data I/O</td>
</tr>
<tr>
<td>UDQM</td>
<td>Upper byte enable</td>
</tr>
<tr>
<td>LDQM</td>
<td>Lower byte enable</td>
</tr>
<tr>
<td>WE</td>
<td>Write enable</td>
</tr>
<tr>
<td>CAS</td>
<td>Column Address Strobe</td>
</tr>
<tr>
<td>RAS</td>
<td>Row Address Strobe</td>
</tr>
<tr>
<td>CKE</td>
<td>Clock Enable</td>
</tr>
<tr>
<td>CLK</td>
<td>Clock</td>
</tr>
</tbody>
</table>

### Additional Information

- Synchronous interface
- Designed for burst-mode operation
- Four separate banks; pipelined operation
Samsung 8M x 16 SDRAM

FUNCTIONAL BLOCK DIAGRAM

- Bank Select
- Row Select
  - Refresh Counter
  - LRAS
- Column Decoder
- Timing Register
- Output Buffer
- I/O Control
- Data Input Register
- Sense AMP
- Latency & Burst Length
- Programming Register
- Timing Register

- Clock (CLK)
- Address (ADD)
- LCKE

- LRAS
- LCAS
- LWE
- LCBR

- LDQM
- LDQMDQi

- CLK
- CKE
- CS
- RAS
- CAS
- WE
- L(U)DQM

*Samsung Electronics reserves the right to change products or specifications without notice.*
### SDRAM: Control Signals

<table>
<thead>
<tr>
<th>RAS</th>
<th>CAS</th>
<th>WE</th>
<th>action</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>NOP</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Load mode register</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Active (select row)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Read (select column, start burst)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Write (select column, start burst)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Terminate Burst</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Precharge (deselect row)</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Auto Refresh</td>
</tr>
</tbody>
</table>

Mode register: selects 1/2/4/8-word bursts, CAS latency, burst on write
SDRAM: Timing with 2-word bursts

Clk

RAS

CAS

WE

Addr

BA

DQ