Memory

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NCTU, Summer 2005

Early Memories

Williams Tube CRT-based random access memory, 1946. Used on the Manchester Mark I. 2048 bits.

Early Memories

Mercury acoustic delay line. Used in the EDASC, 1947. 32 × 17 bits

Early Memories

Magnetic core memory, 1952. IBM.

Early Memories

Magnetic drum memory. 1950s & 60s. Secondary storage.

Modern Memory Choices

<table>
<thead>
<tr>
<th>Family</th>
<th>Programmed Persistence</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mask ROM</td>
<td>at fabrication</td>
</tr>
<tr>
<td>PROM</td>
<td>once</td>
</tr>
<tr>
<td>EPROM</td>
<td>1000s, UV</td>
</tr>
<tr>
<td>FLASH</td>
<td>1000s, block</td>
</tr>
<tr>
<td>EEPROM</td>
<td>1000s, byte</td>
</tr>
<tr>
<td>NVRAM</td>
<td>∞</td>
</tr>
<tr>
<td>SRAM</td>
<td>∞</td>
</tr>
<tr>
<td>DRAM</td>
<td>∞</td>
</tr>
</tbody>
</table>

ROMs

EPROMs

EEPROM and FLASH

Slow write
Fowler-Nordheim Tunneling
EEPROM: bit at a time
FLASH: block at a time
Source: SST
**Static RAM Cell**

Word

Bit

**Standard SRAM: 6264**

19–15, 13–11
10–2, 25–23, 22
20
27
26
28

D[7:0]

Addr[12:0]

8K x 8

Can be very fast:

Cypress sells a 55ns version

Simple, asynchronous interface

**Standard SRAM: 6264**

**Toshiba TC55V16256J 256K x 16**

38–35, 32–29, 16–13, 10–7

D[15:0]

Addr[17:0]

12 or 15 ns access time

Asynchronous interface

UB, LB select bytes

**Toshiba TC55V16256J 256K x 16**

**Dynamic RAM Cell**

Row

Column

Basic problem: Leakage

Solution: Refresh

**Ancient DRAM: 4164**

64K x 1

Apple IIe vintage

9, 13, 10–12, 6, 7, 5

Addr[7:0]

DIN DOUT

14

WE

15

CAS

RAS

**Basic DRAM read and write cycles**

RAS

CAS

Addr

WE

Din

Dout
**SDRAM: Control Signals**

<table>
<thead>
<tr>
<th>RAS</th>
<th>CAS</th>
<th>WE</th>
<th>action</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>NOP</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Load mode register</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Active (select row)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Read (select column, start burst)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Write (select column, start burst)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Terminate Burst</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Precharge (deselect row)</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Auto Refresh</td>
</tr>
</tbody>
</table>

Mode register: selects 1/2/4/8-word bursts, CAS latency, burst on write

**SDRAM: Timing with 2-word bursts**

- **Bank address**
- **Address (multiplexed)**
- **Data I/O**
- **Upper byte enable**
- **Lower byte enable**
- **Write enable**
- **Column Address Strobe**
- **Row Address Strobe**
- **Clock Enable**
- **Clock**

Synchronous interface
Designed for burst-mode operation
Four separate banks; pipelined operation

*Samsung Electronics reserves the right to change products or specification without notice.*