Hardware-Software Interfaces
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Basic Processor Architecture

Typical Processor System

Simple Bus Timing

Strobe vs. Handshake

1982: The IBM PC

The ISA Bus: Memory Read

The ISA Bus: Memory Write

The PC/104 Form Factor: ISA Lives

3.8in
Embedded System Legos. Stack ‘em and go.
Memory-Mapped I/O

- To a processor, everything is memory.
- Peripherals appear as magical memory locations.
- Status registers: when read, report state of peripheral
- Control registers: when written, change state of peripheral

Typical Peripheral: PC Parallel Port

- A Parallel Port Driver

```c
#define DATA 0x378
#define STATUS 0x379
#define CONTROL 0x37A
#define BSY 0x80
#define ACK 0x40
#define OUT 0x20
#define SEL 0x10
#define ERR 0x08
#define STROBE 0x01
#define INVERT (BSY | ACK | OUT | SEL | ERR)
#define MASK (BSY | ACK | OUT | SEL | ERR)
#define NOT READY(x) (!(inb(x) & INVERT) & MASK)

void write_single_character(char c) {
    while (NOT READY(STATUS)) ;
    outb(DATA, c);
    outb(CONTROL, control | STROBE); /* Assert STROBE */
    outb(CONTROL, control); /* Clear STROBE */
}
```

Interrupts and Polling

Two ways to get data from a peripheral:
- Polling: “Are we there yet?”
- Interrupts: Ringing Telephone

Interrupts

Basic idea:
1. Peripheral asserts a processor’s interrupt input
2. Processor temporarily transfers control to interrupt service routine
3. ISR gathers data from peripheral and acknowledges interrupt
4. ISR returns control to previously-executing program

Many Different Interrupts

Processor

Interrupt Polling

Processor receives interrupt
ISR polls all potential interrupt sources

Intel 8259 PIC

Prioritizes incoming requests & notifies processor
ISR reads 8-bit interrupt vector number of winner
IBM PC/AT: two 8259s; became standard