#### Early Memories

**Williams Tube CRT-based random access memory**, 1946. Used on the Manchester Mark I. 2048 bits.

**Mercury acoustic delay line.** Used in the EDASC, 1947. 32 x 17 bits.

**Magnetic core memory**, 1952. IBM.

**Magnetic drum memory.** 1950s & 60s. Secondary storage.

#### Modern Memory Choices

<table>
<thead>
<tr>
<th>Family</th>
<th>Programmed</th>
<th>Persistence</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mask ROM</td>
<td>at fabrication</td>
<td>∞</td>
</tr>
<tr>
<td>PROM</td>
<td>once</td>
<td>∞</td>
</tr>
<tr>
<td>EPROM</td>
<td>1000s, UV</td>
<td>10 years</td>
</tr>
<tr>
<td>FLASH</td>
<td>1000s, block</td>
<td>10 years</td>
</tr>
<tr>
<td>EEPROM</td>
<td>1000s, byte</td>
<td>10 years</td>
</tr>
<tr>
<td>NVRAM</td>
<td>∞</td>
<td>5 years</td>
</tr>
<tr>
<td>SRAM</td>
<td>∞</td>
<td>while powered</td>
</tr>
<tr>
<td>DRAM</td>
<td>∞</td>
<td>64 ms</td>
</tr>
</tbody>
</table>

#### ROMs

8 x 4 ROM

#### EPROMs

EEPROM and FLASH

Slow write
Fowler-Nordheim Tunneling
EEPROM: bit at a time
FLASH: block at a time

Source: SST
### Static RAM Cell

- **Word**
- **Bit**

### Standard SRAM: 6264

- **8K x 8**
- Can be very fast: Cypress sells a 55ns version
- Simple, asynchronous interface

### Standard SRAM: 6264

- **12 or 15 ns access time**
- Asynchronous interface
- UB, LB select bytes

### Toshiba TC55V16256J 256K x 16

- **38–35,32–29,16–13,10–7**
- **23,22,18–21,24–27,42–44,1–5**

### Toshiba TC55V16256J 256K x 16

- **12 or 15 ns access time**
- Asynchronous interface
- UB, LB select bytes

### Dynamic RAM Cell

- **Basic problem: Leakage**
- **Solution: Refresh**

### Ancient DRAM: 4164

- **64K x 1**
- Apple IIe vintage

### Basic DRAM read and write cycles

- **RAS**
- **CAS**
- **Addr**
- **WE**
- **Din**
- **Dout**
**SDRAM: Control Signals**

<table>
<thead>
<tr>
<th>RAS</th>
<th>CAS</th>
<th>WE</th>
<th>action</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>NOP</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Load mode register</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Active (select row)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Read (select column, start burst)</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Write (select column, start burst)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Terminate Burst</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Precharge (deselect row)</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Auto Refresh</td>
</tr>
</tbody>
</table>

Mode register: selects 1/2/4/8-word bursts, CAS latency, burst on write

**SDRAM: Timing with 2-word bursts**

<table>
<thead>
<tr>
<th>Ck</th>
<th>Load</th>
<th>Active</th>
<th>Write</th>
<th>Read</th>
<th>Refresh</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>RAS</td>
<td>CAS</td>
<td>WE</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Page mode read cycle**

**Samsung 8M × 16 SDRAM**

- Bank address
- Address (multiplexed)
- Data I/O
- Upper byte enable
- Lower byte enable
- Write enable
- Column Address Strobe
- Row Address Strobe
- Clock Enable
- Clock

Synchronous interface

Designed for burst-mode operation

Four separate banks; pipelined operation

**Samsung 16 SDRAM**

SDRAM 128Mb E-die (x4, x8, x16) CMOS SDRAM

- Designed for burst-mode operation
- Four separate banks; pipelined operation

*Samsung Electronics reserves the right to change products or specification without notice.*