Spot the Computer
Technical Challenges

Real-time

Complexity

Concurrency

Legacy Languages
Software complexity growing

Size of Typical Embedded System

<table>
<thead>
<tr>
<th>Year</th>
<th>LOC</th>
</tr>
</thead>
<tbody>
<tr>
<td>1985</td>
<td>13 kLOC</td>
</tr>
<tr>
<td>1989</td>
<td>21 kLOC 44 % per year</td>
</tr>
<tr>
<td>1998</td>
<td>1 MLOC</td>
</tr>
<tr>
<td>2000</td>
<td>2 MLOC</td>
</tr>
<tr>
<td>2008</td>
<td>16 MLOC (\approx) Windows NT 4.0</td>
</tr>
<tr>
<td>2010</td>
<td>32 MLOC (\approx) Windows 2000</td>
</tr>
</tbody>
</table>

“Which of the following programming languages have you used for embedded systems in the last 12 months?”

<table>
<thead>
<tr>
<th>Language</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>C</td>
<td>81%</td>
</tr>
<tr>
<td>Assembly</td>
<td>70%</td>
</tr>
<tr>
<td>C++</td>
<td>39%</td>
</tr>
<tr>
<td>Visual Basic</td>
<td>16%</td>
</tr>
<tr>
<td>Java</td>
<td>7%</td>
</tr>
</tbody>
</table>

The Design Challenge

Design optimal device that meets constraints on

- Price
- Functionality
- Performance
- Size
- Power
- Time-to-market
- Maintainability
- Safety
The Time-to-Market Challenge

Typical time-to-market constraint: 8 months
Assuming a constant market ramp, on-time revenue is \( \frac{1}{2} bh = \frac{1}{2} \cdot 2W \cdot W = W^2 \)
and delayed revenue is \( \frac{1}{2} (2W - D)(W - D) \) so fractional revenue loss is

\[
\frac{D(3W - D)}{2W^2} = O(D^2)
\]

Example: when \( W = 26 \) and \( D = 10 \), fraction lost is about 50%. 

Nonrecurring engineering cost: The cost of producing the first one.

![Graph showing the relationship between log unit cost and log volume with two distinct regions: NRE cost dominates and production cost dominates.]

- **NRE cost dominates**
  - Low NRE, high production costs
- **Production cost dominates**
  - High NRE, low production costs
Embedded System Technologies

- Integrated Circuits
- Processing elements
- Design tools
1947: First transistor (Shockley, Bell Labs)

1958: First integrated circuit (Kilby, TI)

1971: First microprocessor (4004: Intel)

Today: six wire layers, 100 nm features
Gordon Moore, 1965: Exponential growth in the number of transistors per IC

Source: Intel
$1000 buys you this many CPS

Source: Ray Kurzweil, *The Age of Spiritual Machines*
1918 Sears Roebuck Catalog

About $100 in today’s dollars.
Spectrum of IC choices

<table>
<thead>
<tr>
<th>Choice</th>
<th>You choose</th>
</tr>
</thead>
<tbody>
<tr>
<td>Full Custom</td>
<td>polygons (Intel)</td>
</tr>
<tr>
<td>ASIC</td>
<td>circuit (Sony)</td>
</tr>
<tr>
<td>Gate Array</td>
<td>wires</td>
</tr>
<tr>
<td>FPGA</td>
<td>logic network</td>
</tr>
<tr>
<td>PLD</td>
<td>logic function</td>
</tr>
<tr>
<td>GP Processor</td>
<td>program (e.g., Pentium)</td>
</tr>
<tr>
<td>SP Processor</td>
<td>program (e.g., DSP)</td>
</tr>
<tr>
<td>Multifunction</td>
<td>settings (e.g., Ethernet)</td>
</tr>
<tr>
<td>Fixed-function</td>
<td>part number (e.g., 74LS00)</td>
</tr>
</tbody>
</table>
### Hardware
- Parallel
- Synchronous
- Logic Gates
- Wire-based communication
- Fixed topology
- Low power
- More detailed
- High NRE
- Faster

### Software
- Sequential
- Asynchronous
- Stored programs
- Memory-based communication
- Highly programmable
- High power
- Less detailed
- No NRE
- Slower
## Design Tools

<table>
<thead>
<tr>
<th>Hardware</th>
<th>Software</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic Synthesis</td>
<td>Compilers</td>
</tr>
<tr>
<td>Place-and-route</td>
<td>Assemblers</td>
</tr>
<tr>
<td>DRC/ERC/LVS</td>
<td>Linkers</td>
</tr>
<tr>
<td>Simulators</td>
<td>Debuggers</td>
</tr>
</tbody>
</table>
Cost of Designs is Rising

1981: 100 designer-months for leading-edge chip
10k transistors, 100 transistors/month

2002: 30 000 designer-months
150M transistors, 5000 transistors/month

Design cost increased from $1M to $300M
Your Nemesis: The XESS XSB-300E
Overview of the XSB Board Circuitry

Components that process video and audio data streams use dedicated buses, while all other components use the shared Peripheral Bus. The audio codec actually connects to both types of buses: it is loaded with configuration data through the Peripheral Bus but it sends and receives digitized audio data through a dedicated bus. The chip-selects for components on the Peripheral Bus are controlled by the FPGA to prevent contention.

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**XC2S300E FPGA**
- 256K x 16 SRAM
- 8M x 16 SDRAM
- 512K x 8 Flash
- 6-channel NTSC video decoder
- 12-bit, 30 MSPS ADC
- 80 MHz, 30-bit video DAC
- 20-bit, 4-input, 1-output stereo codec
- Microphone/line-in/line-out jacks
- 10/100 Ethernet MAC+PHY
- USB 2.0 peripheral port
- Six pushbuttons, DIP switch
- Two LED digits, bargraph
- Three programmable oscillators
- Two expansion headers w/ 75 I/O pins
- Peripheral header w/ 18 I/O pins
- Parallel and Serial port
- Compact Flash interface
- IDE hard disk interface
Class Structure

First half of course: Six Introductory Labs:

1. Count in C on the 7-segment display
2. TV Typewriter in C
3. VHDL system reverse-engineering
4. Sum the contents of a small memory in VHDL
5. Create a simple peripheral
6. Build an OPB interface to off-chip SRAM

Second half project: **Design-your-own**
Custom Project Ideas

Broadly: C + VHDL + peripheral(s)

Digital tone control
Digital sound effects processor
Real-time audio spectrum analyzer
Simple video effects processor
Speech synthesizer
Digital picture frame
Internet radio
Projects from 2004

- MIDI synthesizer
- Line-following robot with video vision
- SAE student vehicle telemetry system
- Stereo video vision system
- Pac-man-like video game
- Internet video camera