Serial Communications  
*CSEE W4840*  
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### Early Serial Communication

- Defined in early 1960s
- Serial, Asynchronous, Full-duplex, Voltage-based, point-to-point, 100 ft+ cables
- **RS-232**
  - Defined in early 1960s
  - Serial, Asynchronous, Full-duplex, Voltage-based, point-to-point, 100 ft+ cables
  - +12V
  - +3V
  - -3V
  - -12V
  - Idle Start LSB B1 B2 B3 B4 B5 B6 Parity Stop
  - Tx

### RS-232 Signals

<table>
<thead>
<tr>
<th>Signal DB-9 DTE</th>
<th>Meaning DCE</th>
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<tbody>
<tr>
<td>RxD 2</td>
<td>Data received by DTE</td>
</tr>
<tr>
<td>TxD 3</td>
<td>Data sent by DTE</td>
</tr>
<tr>
<td>SG 5</td>
<td>Ground</td>
</tr>
<tr>
<td>DSR 6</td>
<td>Data Set Ready (I'm alive)</td>
</tr>
<tr>
<td>DTR 4</td>
<td>Data Terminal Ready (me, too)</td>
</tr>
<tr>
<td>DCD 1</td>
<td>Carrier Detect (hear a carrier)</td>
</tr>
<tr>
<td>RTS 7</td>
<td>Request To Send (Yo?)</td>
</tr>
<tr>
<td>CTS 8</td>
<td>Clear To Send (Yo!)</td>
</tr>
<tr>
<td>RI 9</td>
<td>Ring Indicator</td>
</tr>
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### Receiving RS-232

- Most UARTs actually use 16 × clocks

### Variants

- Parity bit: (Even = true when even number of 1s)
- Two stop bits:

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### Baud Rate

- Baud: bits per second
- **Baud Application**
  - 110 ASR-33 Teletype
  - 300 Early acoustic modems
  - 1200 Direct-coupled modems c. 1980
  - 2400 Modems c. 1990
  - 9600 Serial terminals
  - 19200
  - 38400 Typical maximum

### Physical Variants

- Connectors: DB-25, DB-9, Mini DIN-8
- **RS-422**: Differential signaling
- **RS-485**: Bus-like
OPB UART Lite

Serial port peripheral for the Microblaze
Full duplex operation
16-character transmit and receive FIFOs
Parameters that can be set at build time:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Base Address</td>
<td>0xFEFF0100</td>
</tr>
<tr>
<td>High Address</td>
<td>0xFEFF01FF</td>
</tr>
<tr>
<td>Baud Rate</td>
<td>9600</td>
</tr>
<tr>
<td>Bits per frame</td>
<td>8</td>
</tr>
<tr>
<td>Parity</td>
<td>None</td>
</tr>
</tbody>
</table>

OPB UART Lite Registers

<table>
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<tr>
<th>Address</th>
<th>Role</th>
</tr>
</thead>
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<tr>
<td>0xFEFF0100</td>
<td>Read characters from Receive FIFO</td>
</tr>
<tr>
<td>0xFEFF0104</td>
<td>Write characters to Receive FIFO</td>
</tr>
<tr>
<td>0xFEFF0108</td>
<td>Status register (read only)</td>
</tr>
<tr>
<td>0xFEFF010C</td>
<td>Control register (write only)</td>
</tr>
</tbody>
</table>

Status and Control Registers

<table>
<thead>
<tr>
<th>Bit</th>
<th>Status</th>
<th>Control</th>
</tr>
</thead>
<tbody>
<tr>
<td>24</td>
<td>Parity Error</td>
<td>-</td>
</tr>
<tr>
<td>25</td>
<td>Framing Error</td>
<td>-</td>
</tr>
<tr>
<td>26</td>
<td>Overrun Error</td>
<td>-</td>
</tr>
<tr>
<td>27</td>
<td>Interrupts</td>
<td>Enable Interrupts</td>
</tr>
<tr>
<td>28</td>
<td>Tx buffer full</td>
<td>-</td>
</tr>
<tr>
<td>29</td>
<td>Tx buffer empty</td>
<td>-</td>
</tr>
<tr>
<td>30</td>
<td>Rx buffer full</td>
<td>Clear Rx buffer</td>
</tr>
<tr>
<td>31</td>
<td>Rx buffer non-empty</td>
<td>Clear Tx buffer</td>
</tr>
</tbody>
</table>

Non-empty Rx buffer or emptying of Tx buffer generates an interrupt.

The I²C Bus

Philips invented the Inter-IC bus c. 1980 as a very cheap way to communicate slowly among chips
E.g., good for setting control registers
100, 400, and 3400 KHz bitrates

SCL: Clock, generated by a single master
SDA: Data, controlled by either master or slaves

I²C Bus Transaction

SCL: Clock
SDA: Data

USB: Universal Serial Bus

1.5 Mbps, 12 Mbps, and 480 Mbps (USB 2.0)
Point-to-point, differential, twisted pair
3–5m maximum cable length

USB Connectors

Series "A" Connectors | Series "B" Connectors
--- | ---
- Series "A" plugs are always oriented upstream towards the Host System | - Series "B" plugs are always oriented downstream towards the USB Device

"A" Plugs (From the USB Device) | "B" Plugs (From the USB Device)
--- | ---
| "A" Receptacles (Downstream Only) from the USB Host or Hub | "B" Receptacles (Upstream Only to the USB Device or Hub)

USB signaling

NRZI: 0 = toggle, 1 = no change
Bit stuffing: 0 automatically inserted after six consecutive 1s

USB Packets

Always start with SYNC
Then 4-bit type, 4-bit type complemented
2 bits distinguish Token, Data, Handshake, and Special, other two bits select sub-types
Then data, depending on packet type
Data checked using a CRC
Addresses (1-128) assigned by bus master, each with 16 possible endpoints
USB Bus Protocol

Polled bus: host initiates all transfers. Most transactions involve three packets:
- “Token” packet from host requesting data
- Data packet from target
- Acknowledge from host

Supports both streams of bytes and structured messages (e.g., control changes).

USB Data Flow Types

- Control: For configuration, etc.
- Bulk Data: Arbitrary data stream: bursty
- Interrupt Data: Timely, reliable delivery of data. Usually events.
- Isochronous Data: For streaming real-time transfer: renegotiated bandwidth and latency

Layered Architecture

Host
Interconnect
Physical Device

Client SW

Function Layer

USB System SW

USB Logical Device

USB Device SW

USB Bus Interface

Function Layer

Actual communications flow

Logical communications flow

Implementation Focus Area

USB: Flash Card Device

USB: Mouse Device

The CY7C68001 USB interface

The CY7C68001 software interface

Operates as a peripheral (i.e., not a host)
Operates at 12 or 480 Mbps speeds
Control endpoint 0
Four other user-configurable endpoints
4 kB FIFO buffer
500 bytes of descriptor RAM (Vendor, Product)
I²C bus interface for configuration from EEPROM
(Unused on the XSB board—processor must configure)

Five memory locations: one for each FIFO, one for control registers
Internal registers written by first applying address to control register, then reading or writing data to control register.
33 different configuration registers, including 500-byte descriptor “register”