 YOUR NAME: _____

Midterm

CSEE W3827 - Fundamentals of Computer Systems — Oct. 20, 2009
Fall 2008 — Prof. Rubenstein

This midterm contains 4 questions, and totals 100 points. To get full credit you must answer all questions. **BOOKS AND NOTES ARE PERMITTED, BUT ELECTRONIC DEVICES ARE NOT!** The time allowed is 75 minutes.

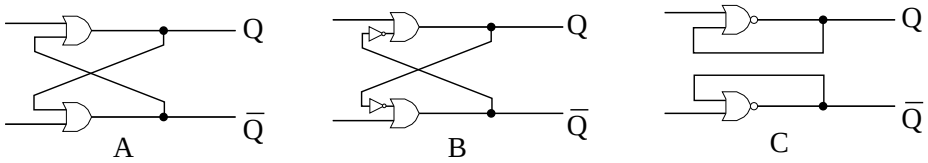
Please answer all questions **in the blue book**, using a **separate** page for each question. **Show all work!** We are not just looking for the right answer, but also how you reached the right answer.

If you remember to write your name on your exam, and turn in your exam, then you may solve problem 2b on the exam using the included figure.

1. (20 pts) Answer the following questions, using no more than a sentence for each part.

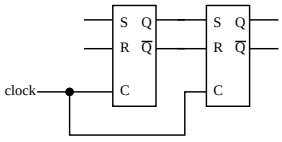
   (a) (3 pts) What is the value of 11010, if it represents a binary number in 2's-complement form?

   (b) (3 pts) If $A = 101101000101010010010$ represents a number in 2's complement form and is added to itself, is there an overflow? Explain for more than just 1 point credit.



   (c) (9 pts) Can the three proposed designs above (A,B,C) be used as a latch that implements 3 modes: set ($Q = 1, \bar{Q} = 0$), reset ($Q = 0, \bar{Q} = 1$), and hold value? For each design that can, indicate the inputs that produce the various modes. Otherwise, briefly explain what the design problem is with the latch problem. (only 1 point for guessing right without describing inputs or explanation).

   (d) (2 pts) Latches have input combinations that allow them to be set, reset, or hold their current value. Why don't latches have an input combination that complements their current value?



   (e) (3 pts) The flip-flop, pictured above is built from two S-R latches. What's wrong with this flip-flop?

2. (20 points) The circuit depicted below in Figure 1(a), takes 4 inputs, I_0, I_1, I_2, I_3 and returns output O which equals a 1 if exactly 1 of the input equals 1 and the other inputs equal 0. Otherwise, the output equals 0.

(a) $J4$ circuit (b) $J10$ circuit

Figure 1:

(a) (10 pts) Design this circuit using the PLA provided below in Figure 2.

(b) (10 pts) Show how to combine several of these $J4$ circuits to emulate a similar $J10$ circuit, depicted in Figure 1(b), that equals 1 when exactly one of its 10 inputs equals 1, and equals 0 otherwise.

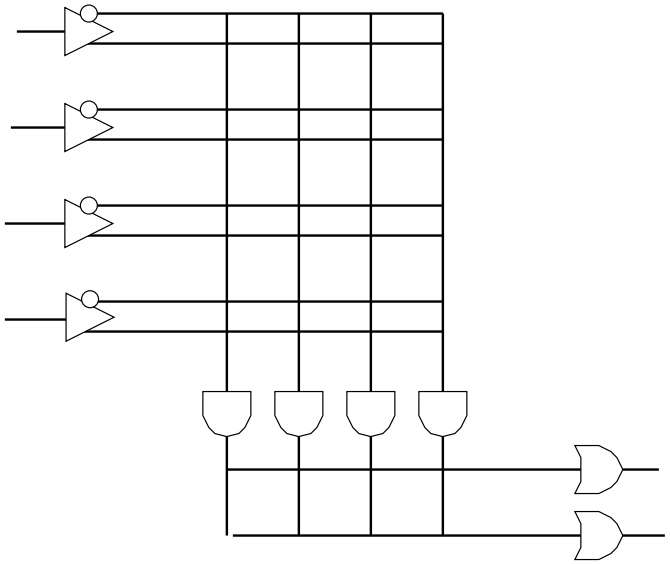


Figure 2: The PLA to use.

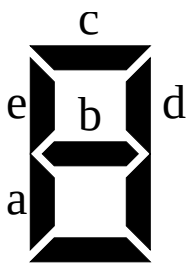
3. (30 pts) In this problem, you will build a 7-segment reader, which takes a 7-segment encoding of a number and converts it to its binary value. Specifically, given the 4 inputs depicted below left, a,b,c,d,e, which equal 1 when the respective segment is active, you must convert this input to the appropriate 4-bit binary value. For instance, input $abcde = 10111$ corresponds to the value 0 (0000), and $abcde = 01011$ corresponds to the value 4 (0100), and $abcde = 11111$ corresponds to the value 8 (1000).

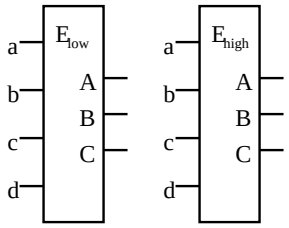
   (a) (15 pts) Begin by building a 4-to-3 encoder in the middle figure, called E_{low} that assumes that $e = 0$ and takes inputs a, b, c, d and converts the code to binary outputs A, B, C. Note that when segment $e = 0$, the value to be output in binary is less than 8. **Represent your answer in algebraic, sum-of-products form, but simplify as much as possible in this form!**

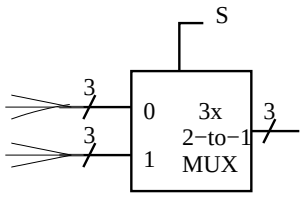
   (b) (5 pts) Next, build a 4-to-3 encoder, also depicted in the middle figure, called E_{high} that assumes that $e = 1$ and takes inputs a, b, c, d and converts the input to the 3-bit binary representation modulo 8 (i.e., leaving off the high order bit so that 8 is 000 and 9 is 001). **Represent your answer in algebraic, sum-of-products form, but simplify as much as possible in this form!**

   (c) (10 pts) Using three 2-to-1 MUX's in parallel (as depicted in the figure on the right), your E_{low} and E_{high} circuits, and any additional AND,OR, and NOT gates you think are needed, design the complete circuit that takes in 5 inputs, a, b, c, d, e, and outputs the 4-bit binary representation of the number being displayed by the 7-segment representation.

   (Hint: to produce the high-order bit, note that the bit is only set when the 7-segment display is showing either 8 or 9, and that only 8 and 9 have b, c, d, e all set to 1.







4. (30 pts) A signal is being received across a noisy channel. To compensate, a rule is applied that a signal must last at least two clock cycles to be considered valid. If a signal changes only holds a particular value for a single clock cycle, that value is ignored.

   More specifically, let $I(t)$ be the input at time t, $O(t)$ the output at time t Then

   - If $I(t) = I(t-1)$ then $O(t) = I(t)$
   - If $I(t) \neq I(t-1)$ then $O(t) = O(t-1)$

   Below is an example

time	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
$I(t)$	0	0	0	1	0	0	1	0	1	1	1	0	1	0	1	0	0	1	0	1
$O(t)$	X	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0

   (a) (15 points) Draw the state machine that implements the above filter.

   (b) (15 points) Build the sequential circuit using JK flip-flops. The JK flip-flop excitation table is below, where $\neg A(t-1)$ means $\overline{A(t-1)}$.

JK flip-flop		
J-In	K-In	$A(t)$
0	0	$A(t-1)$
0	1	0
1	0	1
1	1	$\neg A(t-1)$