WEEK #1: September 8-10

Introduction.

Course overview, recent trends, modern digital design and systems.

Combinational Logic: Quick Review.

Boolean representations, two-level/multi-level logic, structured blocks.

Sequential Logic: Registers and Shift-Register Counters.

Johnson counters, linear feedback shift-registers (LFSR's) for pseudo-random number generation.

WEEK #2: September 15-17

Sequential Logic: Clocked State Machine Design.

General counter design procedure. State machine structures: Moore vs. Mealy.
Controller design procedure. Complex modelling case studies, deriving a specification.

WEEK #3: September 22-24

Introduction to VHDL. Combinational Modelling.

Basic combinational modelling examples. Formal syntax. Entities and architectures.
Libraries and packages. Structural, dataflow and behavioral modelling.
Selected and conditional signal assignment statements, for-generate statements, multi-bit operations.

WEEK #4: September 29-October 1

Sequential Logic: Iterative Circuits.

Unrolling FSM's: designing fast combinational pattern detectors, comparators.

Sequential Optimization Techniques and Case Studies.

Optimal state encoding; state minimization; controller partitioning; real-world design examples.

WEEK #5: October 6-8

Arithmetic Circuits (1): Basic Combinational Adders.

Ripple-carry adder review. Von Neumann's average worst-case carry-chain analysis.

Arithmetic Circuits (2): Advanced Combinational Adders.

High-Speed Adders: carry-lookahead (CLA), carry-select, carry-skip, conditional sum.
Parallel-prefix tree adders: Kogge-Stone, Brent-Kung.
Tradeoffs between delay, area and power. Parallelism and speculation strategies.

WEEK #6: October 13-15

Arithmetic Circuits (3): Combinational Array Multipliers.

Basic version. Performance optimization using carry-save addition.

Low-Power Digital Optimization Techniques.

Recent techniques: combinational logic transformations; FSM partitioning; bus encoding.

WEEK #7: October 20-22

Sequential VHDL.

Modeling flip-flops, registers, state machines: templates and practical strategies.

Fault-Tolerance and Reliability (1): Error Detection and Correction.

Error detection/correction: Hamming and CRC codes, unordered codes (Berger, m-of-n).

WEEK #8: October 27-29

Fault-Tolerance and Reliability (2): Soft Error Mitigation.

Recent approaches to "hardening" designs against soft errors (due to cosmic rays).

Introduction to Asynchronous Design: Overview.

Processes and communication: handshaking protocols, data encoding, completion detection.
Modelling concurrent systems using Petri nets.

WEEK #9: November 3-5 [NO CLASS 11/3: Election Day]

Asynchronous Design: Controllers.

Motivation. Clockless controller synthesis: "burst-mode" specifications.
The Columbia "MINIMALIST" CAD tool, case studies and tutorial.

MIDTERM: THURSDAY, NOVEMBER 5 (in class).

WEEK #10: November 10-12

Architectural Synthesis: Register-Transfer Level (RTL) Design.

Algorithmic State Machine charts (ASM's).
Specification and design procedure for large complex digital systems. Detailed case study.

WEEK #11: November 17-19

Architectural Synthesis: Register-Transfer Level (RTL) Design.

Detailed case study (concl.). Timing issues. Optimizations: resource sharing, scheduling.
System-level performance tuning, area/delay tradeoffs.

Asynchronous Design: High-Speed Pipelines.

MOUSETRAP pipelines. Handling non-linear topologies.

WEEK #12: November 24-26 [NO CLASS 11/26: Thanksgiving]

Asynchronous Design: Introduction to Hazard-Free Combinational Logic.

Multiple-input changes. Hazard-free two-level logic minimization. Multi-level logic.

WEEK #13: December 1-3

Advanced Topics (1): FPGA Internals.

Actel and Xilinx case studies. Gate-level industrial structures.

Advanced Topics (2): Synchronous Timing Issues and Challenges.

Synchronizers, metastability, synchronization failure, practical solutions.

WEEK #14: December 8-10

Advanced Topics (3): Introduction to Floating Point Arithmetic.

Number representation, floating-point unit design.

FINAL EXAM (TENTATIVE). Thursday, December 17, 1:10-4:00 p.m. (Room: TBA)