WEEK #1: January 20-22

Introduction.
   Course overview, recent trends, modern digital design and systems.

Combination Logic: Quick Review.
   Boolean representations, two-level/multi-level logic, structured blocks. Finite bases.

Sequential Logic: Latches/Flipflops (Quick Overview).

WEEK #2: January 27-29

Sequential Logic: Registers and Shift-Register Counters.
   Johnson counters, linear feedback shift-registers (LFSR’s) for pseudo-random number generation.

Sequential Logic: Clocked State Machine Design.
   Controller design procedure: Moore and Moore machines. Timing issues.
   Sequential optimization: optimal state encoding, state minimization.

WEEK #3: February 3-5

Sequential Logic: Clocked State Machine Design.
   Complex modeling case studies, deriving a specification.

Sequential Logic: Iterative Circuits.
   Unrolling FSM’s: designing fast combinational pattern detectors, comparators.

Advanced Topics (1): FPGA Internals.
   Actel and Xilinx case studies. Gate-level industrial structures.

Introduction to VHDL. Combinational Modeling.
   Basic combinational modeling examples. Formal syntax. Entities and architectures.

WEEK #4: February 10-12

Introduction to VHDL. Combinational Modeling (cont.).
   Libraries and packages. Structural, dataflow and behavioral modeling.
   Selected and conditional signal assignment statements, for-generate statements.
   Multi-bit operations; delta delays, simulation semantics.

Arithmetic Circuits (1): Basic Combinational Adders.
   Ripple-carry adder review. Von Neumann’s average worst-case carry-chain analysis.

WEEK #5: February 17-19

Arithmetic Circuits (2): Advanced Combinational Adders.
   High-Speed Adders: carry-select, conditional sum, carry-skip, carry-lookahead.
   Tradeoffs between delay, area and power. Strategies: parallelism vs. speculation.
   Introduction to ternary/higher-radix arithmetic.

WEEK #6: February 24-26

Arithmetic Circuits (2): Advanced Combinational Adders (cont.).
   Parallel-prefix (tree) adders: Kogge-Stone, Brent-Kung. Hybrid structures, saturating arithmetic.

Sequential VHDL.
   Modeling flip-flops, registers, state machines: templates and practical strategies.

Arithmetic Circuits (3): Combinational Array Multipliers.
   Basic version. Performance optimization using carry-save addition.
WEEK #7: March 3-5

Low-Power Digital Techniques (1).
Sequential precomputation architectures.

Low-Power Digital Techniques (2).
Low-power bus encoding.

WEEK #8: March 10-12

MIDTERM: TUESDAY, MARCH 10 (in class).

Fault-Tolerance and Reliability: Error Detection and Correction.
Parity, Hamming, and two-dimensional (product) codes.

WEEK OF MARCH 16–MARCH 20: SPRING BREAK.

WEEK #9: March 24-26

Fault-Tolerance and Reliability: Error Detection and Correction (cont.).
Cyclic redundancy check (CRC) codes.

Asynchronous Design: Overview.
Motivation and industrial trends. Handshaking protocols, data encoding, completion detection.

Asynchronous Design: Controllers.
Clockless controller synthesis: “burst-mode” specifications.
The Columbia MINIMALIST CAD tool, case studies and tutorial.

WEEK #10: March 31-April 2

Algorithmic State Machine charts (ASM’s).
Specification and design procedure for large complex digital systems. Detailed case study.

WEEK #11: April 7-9

Architectural Synthesis: Register-Transfer Level (RTL) Design (cont.).

Digression: Floating Point Arithmetic.
Single- and double-precision representation. FP-integer conversion, FP multiplication.
Special cases: overflow, zero, infinity, rounding issues, advanced modes.

WEEK #12: April 14-16

Architectural Synthesis: Register-Transfer Level (RTL) Design (cont.).
System-level performance tuning, parallel vs. serial operation, area/delay/power tradeoffs.

WEEK #13: April 21-23

Asynchronous Design: High-Speed Pipelines.
MOUSETRAP pipelines. Handling non-linear topologies, applications.

Crossing clock domains: synchronizers, metastability, synchronization failure, practical solutions.

WEEK #14: April 28-30

Introduction to Testability and Design-for-Test.
Fault models, stuck-at and delay faults, scan structures, built-in self-test (BIST), synthesis-for-testability.

Advanced Topics (3): Soft Error Mitigation.
Recent techniques for robustness to transient failures (due to cosmic rays).

FINAL EXAM (TENTATIVE). Tuesday, May 12, 4:10-7:00 p.m. (Room: TBA)