

CSEE 4823 Advanced Logic Design

Handout: Lecture #9

10/4/11



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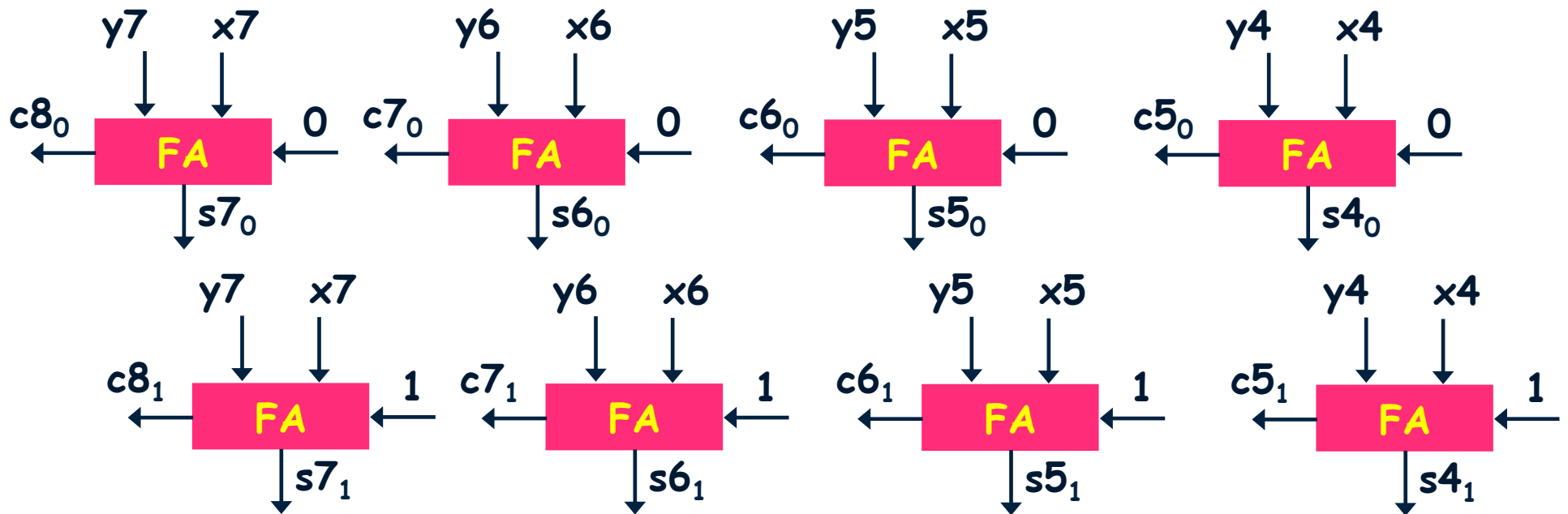
New York, NY, USA

Conditional Sum Adders



8-Bit Conditional Sum Adder: Level 1

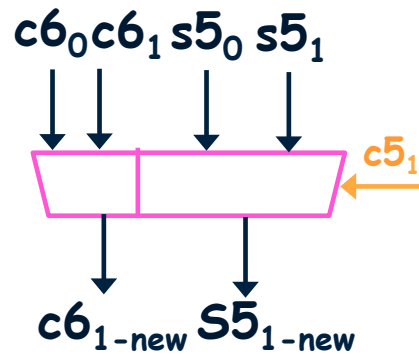
Deriving Design for Bits 4-7 = typical case (i.e. not near right side)



8-Bit Conditional Sum Adder:

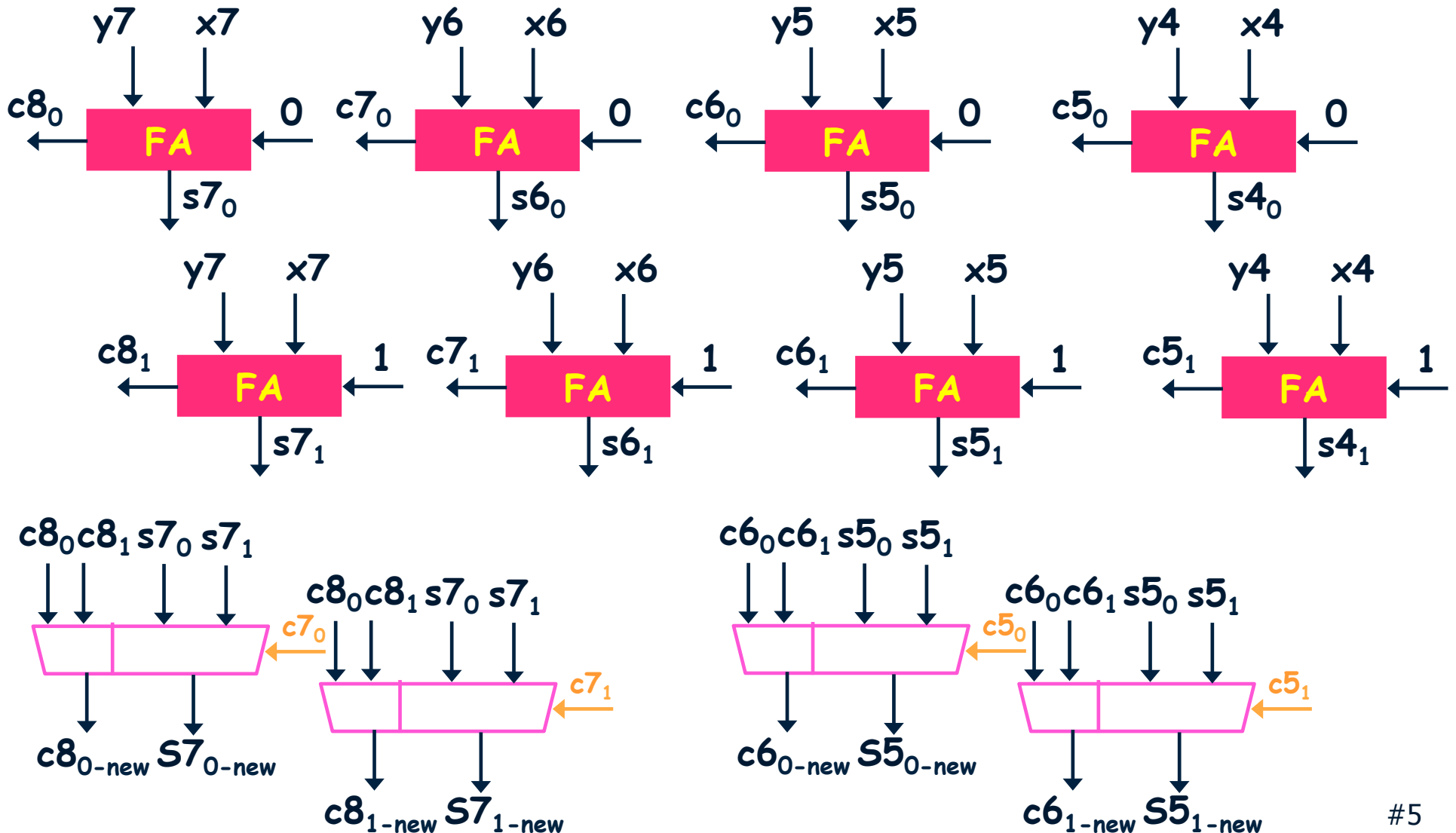
Deriving Design for Bits 4-7 = typical case (i.e. not near right side)

Notation: two 2-to-1 MUXes with the same select signal (c_{5-1})



8-Bit Conditional Sum Adder: Levels 1 & 2

Deriving Design for Bits 4-7 = typical case (i.e. not near right side)



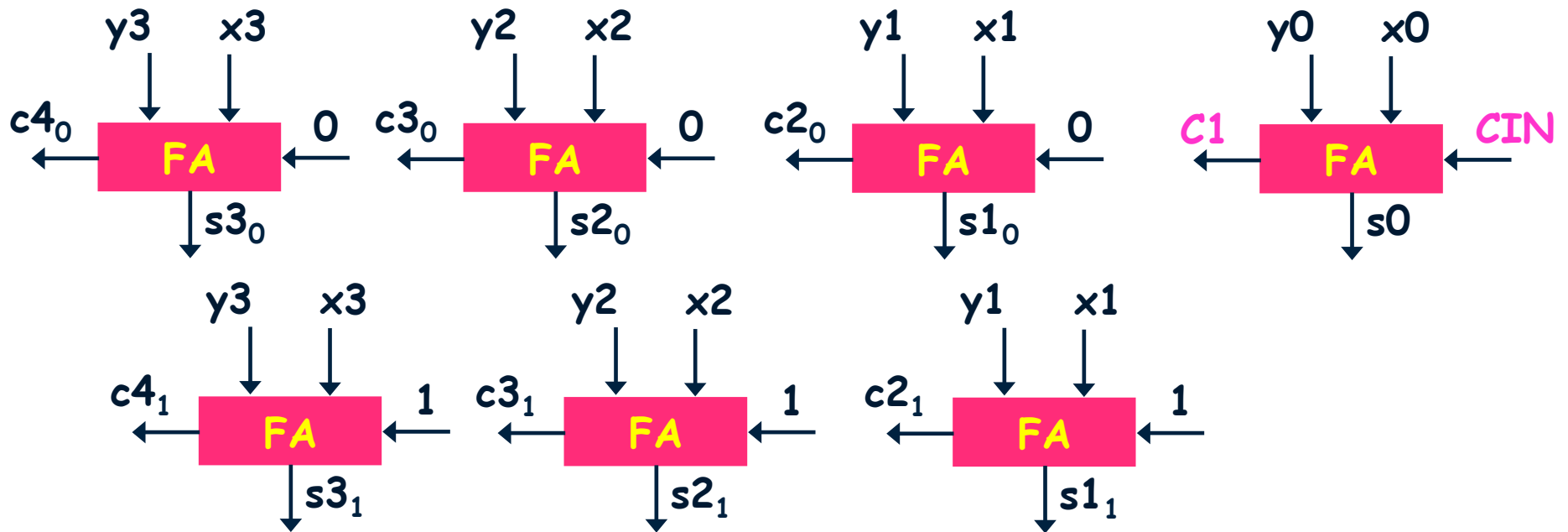
8-Bit Conditional Sum Adder: Levels 1 to 4

Deriving Design for Bits 4-7 = typical case (i.e. not near right side)

Levels 1 through 4 (complete): see Conditional Sum Adder handout

8-Bit Conditional Sum Adder: Level 1

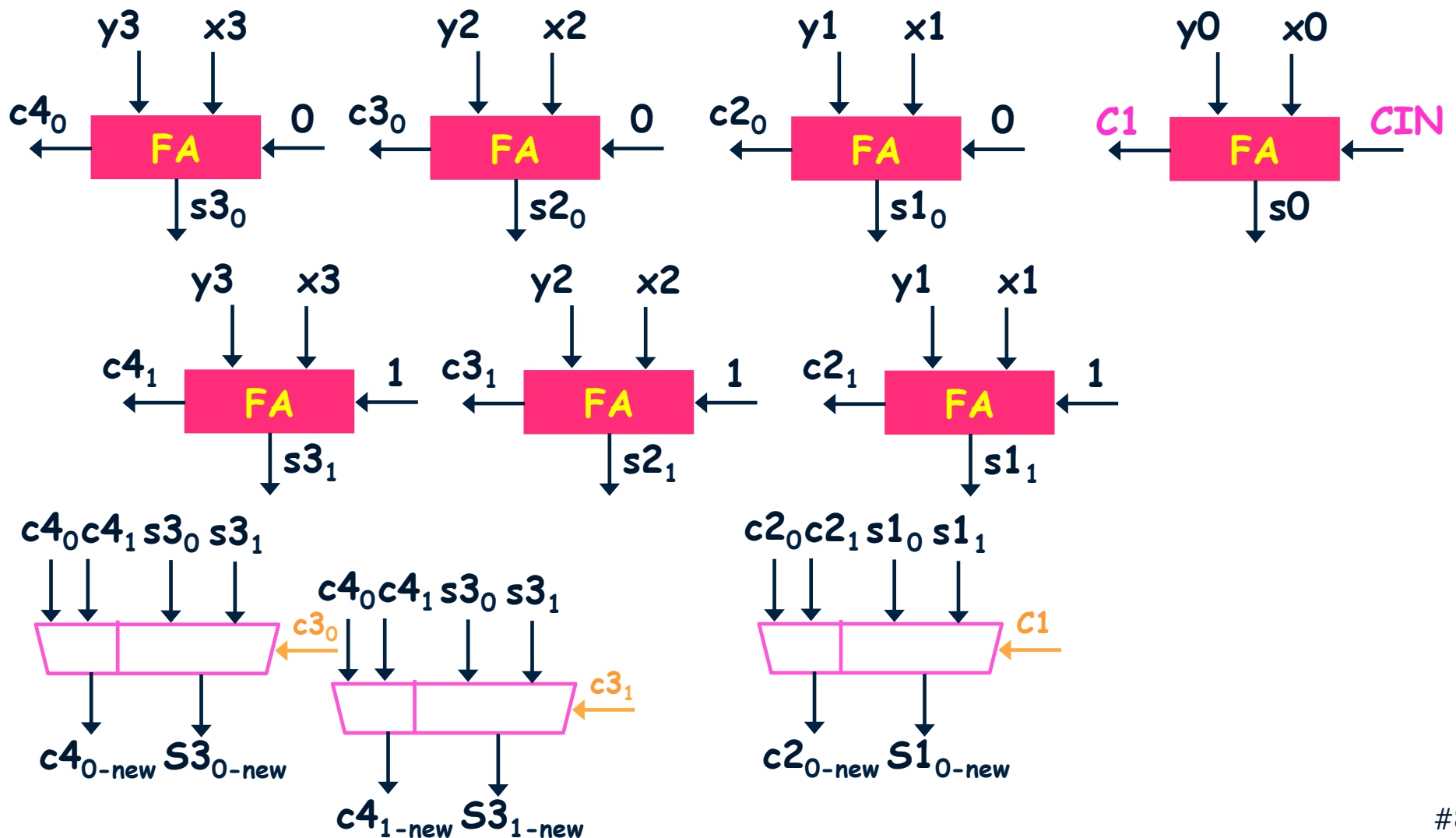
Deriving Design for Bits 0-3 = special case (i.e. at right side)



Note: no speculation of two options in bit 0, since CIN is known.

8-Bit Conditional Sum Adder: Level 1 & 2

Deriving Design for Bits 0-3 = special case (i.e. at right side)



8-Bit Conditional Sum Adder: Levels 1 to 3

Deriving Design for Bits 0-3 = special case (i.e. at right side)

Levels 1 through 3 (complete): see Conditional Sum Adder handout

8-Bit Conditional Sum Adder: Final Design

...see Conditional Sum Adder handout