

CSEE 4823 Advanced Logic Design

Handout: Lecture #10

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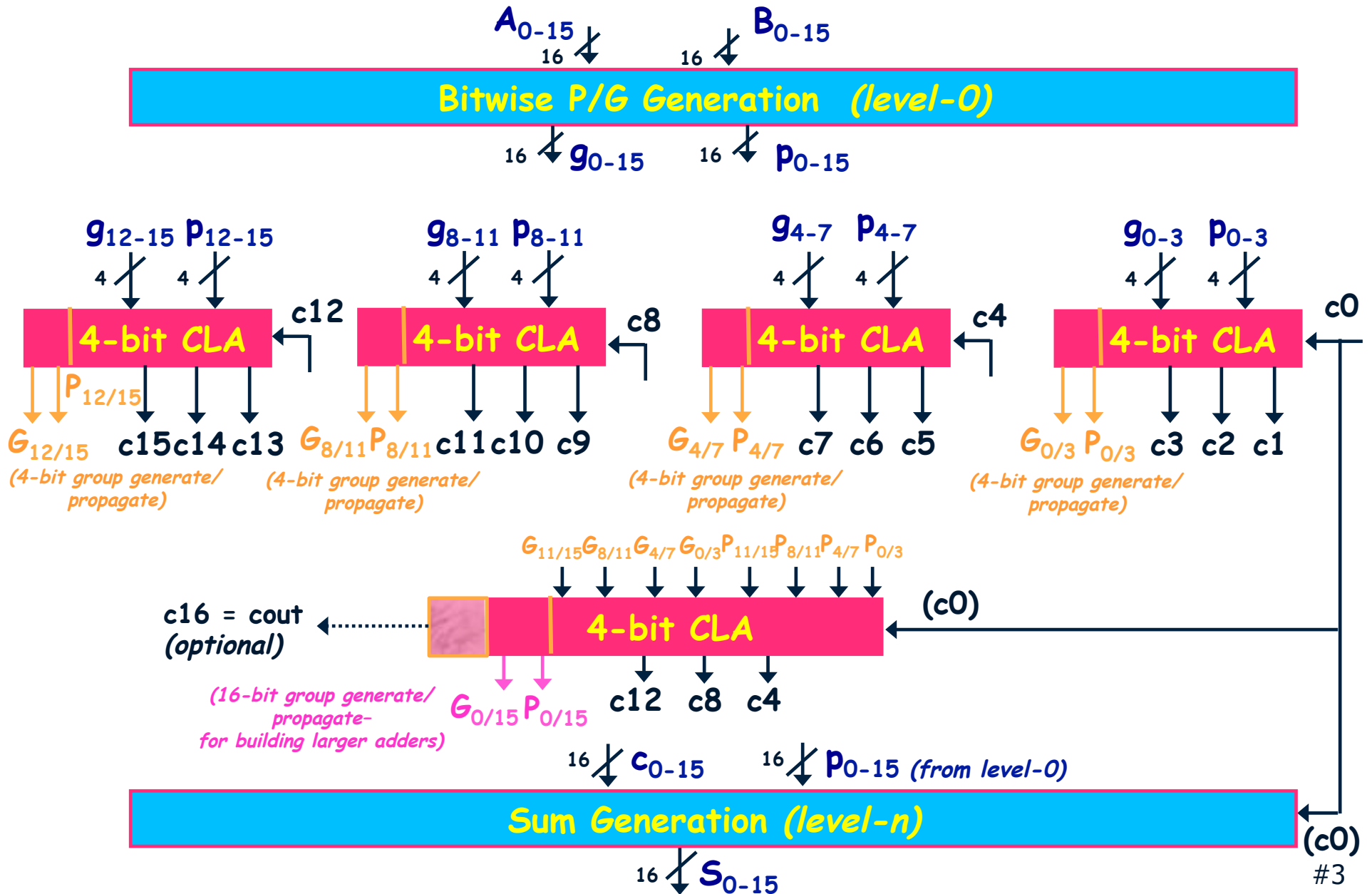
Columbia University

New York, NY, USA

Carry-Lookahead Adders (CLA' s) ***(hierarchical)***



16-Bit Hierarchical CLA: Overall Architecture



16-Bit Hierarchical CLA: Details of Cell Design

Level-0: Bitwise P/G Generation – logic equations for bit i

$$p_i = a_i \text{ XOR } b_i$$

$$g_i = a_i b_i$$

4-Bit CLA Cell: one example = bits 0-3 – logic equations

Carry Bits:

$$c_1 = g_0 + p_0 c_0$$

$$c_2 = g_1 + p_1 g_0 + p_1 p_0 c_0$$

$$c_3 = g_2 + p_2 g_1 + p_2 p_1 g_0 + p_2 p_1 p_0 c_0$$

Group P & G Bits:

$$G_{0/3} = g_3 + p_3 g_2 + p_3 p_2 g_1 + p_3 p_2 p_1 g_0$$

$$P_{0/3} = p_3 p_2 p_1 p_0$$

Level-N: Sum Generation – logic equations for bit i

$$s_i = p_i \text{ XOR } c_i$$