

# Compositional Dataflow Circuits

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```
gcd(a, b) =  
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    a  
  else if a < b  
    gcd(a, b - a)  
  else  
    gcd(a - b, b)
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else if  $a < b$

$\text{gcd}(a, b - a)$

else

$\text{gcd}(a - b, b)$

$a$



$b$



$\text{gcd}(a, b) =$

**if  $a = b$**

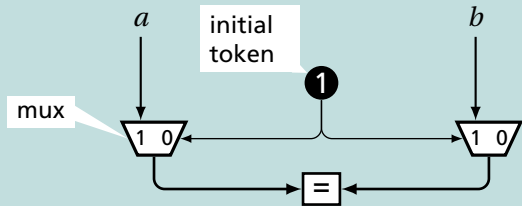
$a$

else if  $a < b$

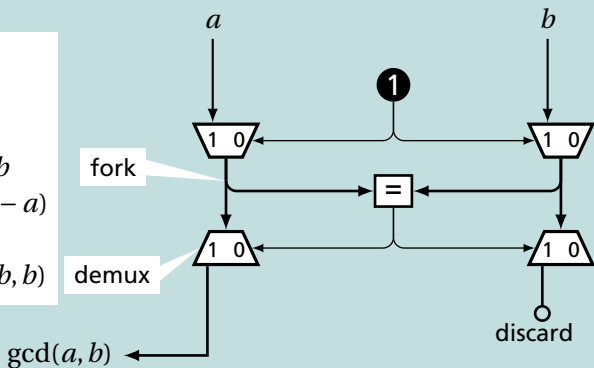
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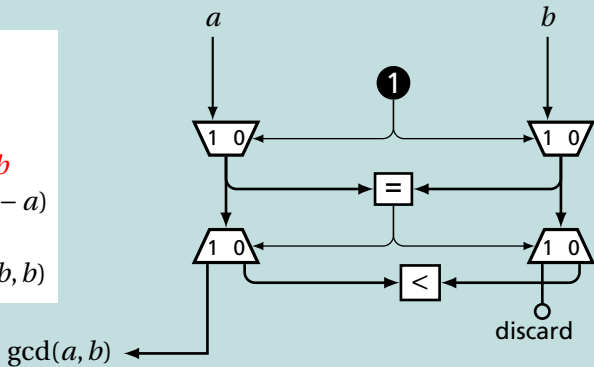
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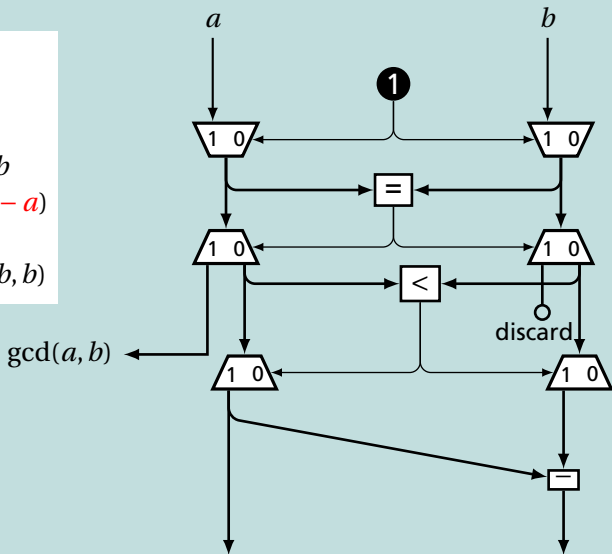
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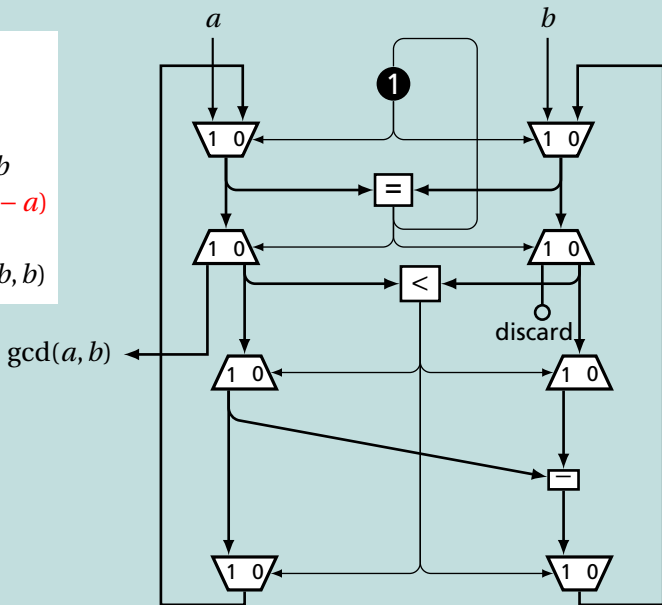
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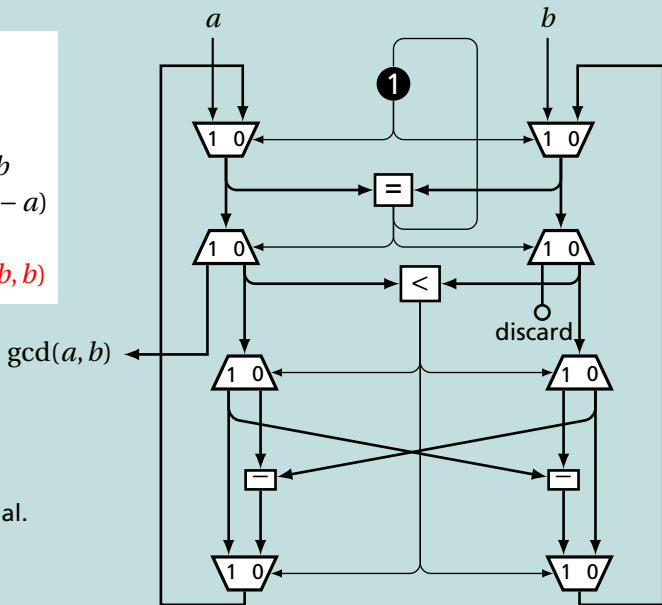


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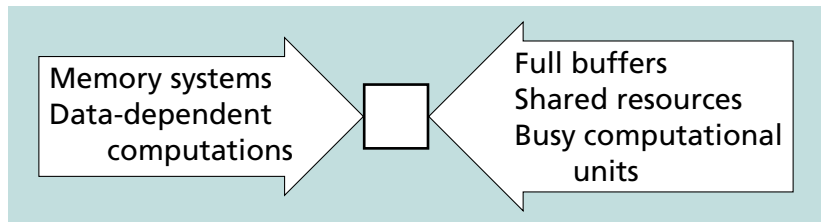


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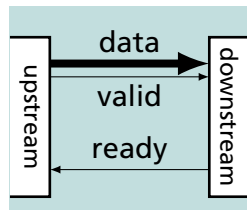
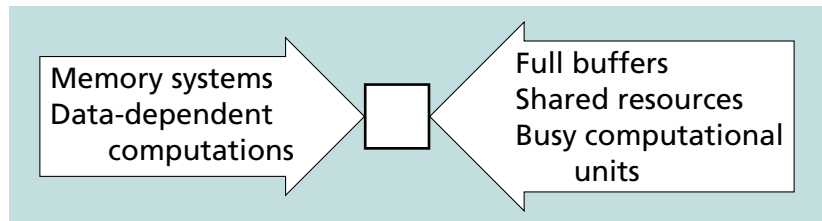
# Patience Through Handshaking

Want *patient* blocks to handle delays from



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| valid | ready | Meaning              |
|-------|-------|----------------------|
| 1     | 1     | Token transferred    |
| 1     | 0     | Token valid; held    |
| 0     | –     | No token to transfer |

Latency-insensitive Design (Carloni et al.)

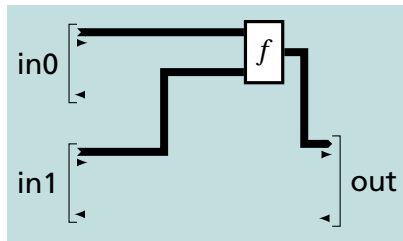
Elastic Circuits (Cortadella et al.)

FIFOs with backpressure

# Combinational Function Block

Strict/Unit Rate:

All input tokens required to produce an output



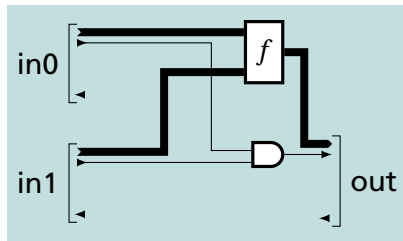
Datapath

Combinational function ignores flow control

# Combinational Function Block

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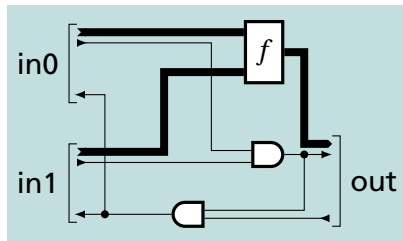
Valid network

Output valid if both inputs are valid

# Combinational Function Block

Strict/Unit Rate:

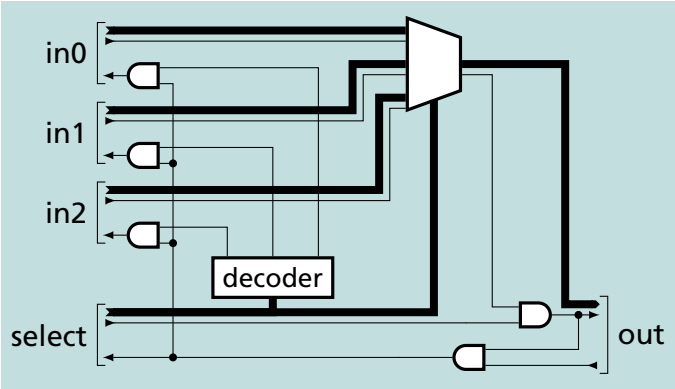
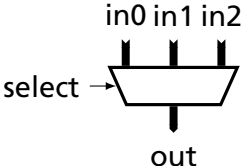
All input tokens required to produce an output



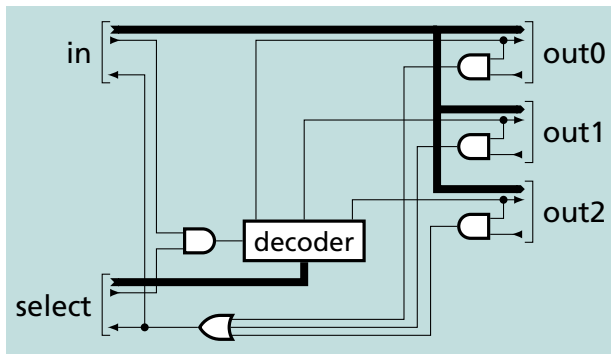
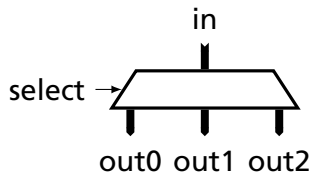
Ready network

Input tokens consumed if output token is consumed  
(output is valid and ready)

# Multiplexer Block

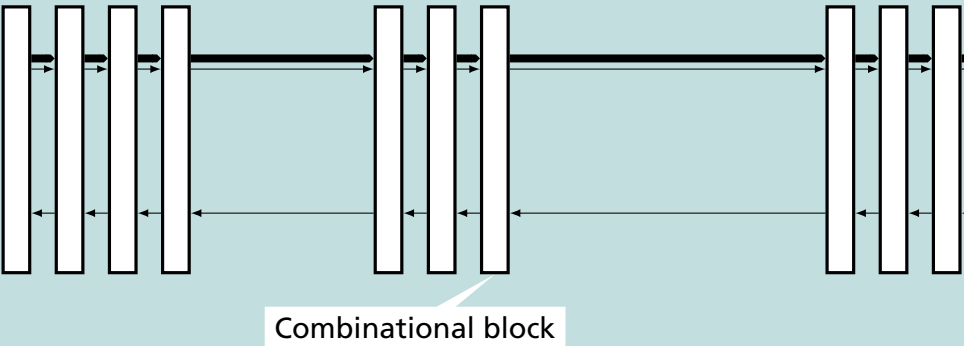


# Demultiplexer Block

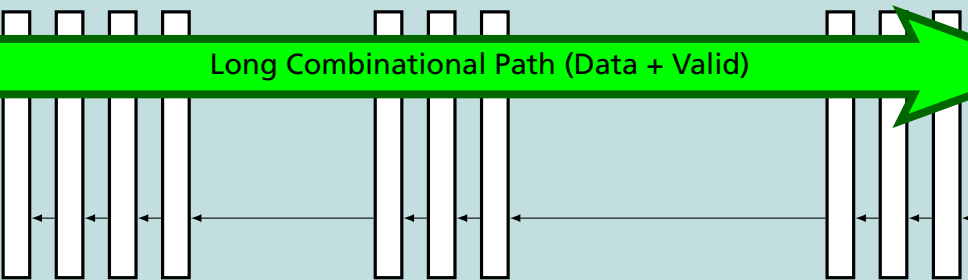




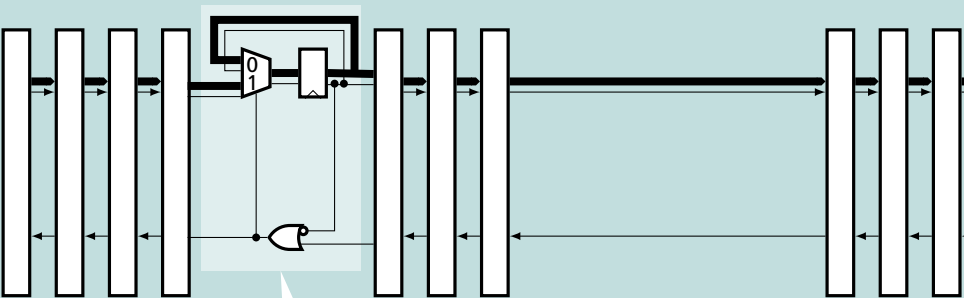
## Buffering a Linear Pipeline (Point 1/4)



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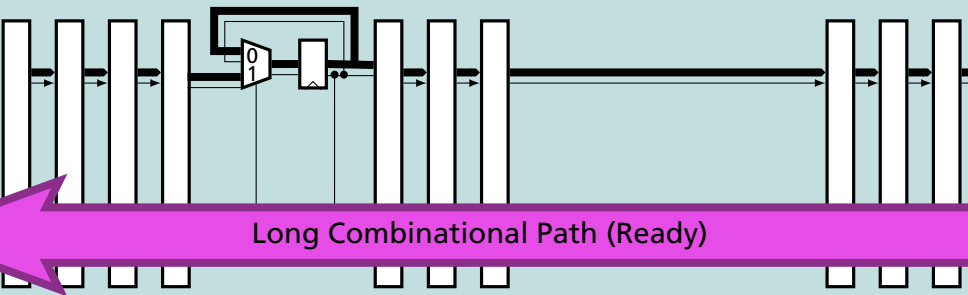


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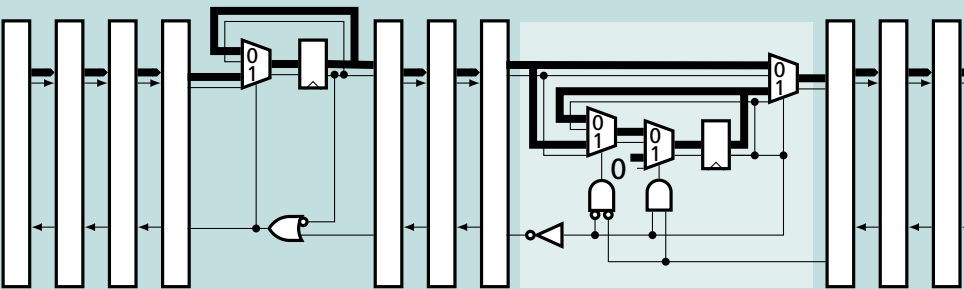


Data buffer:  
Pipeline register  
with valid, enable

## Buffering a Linear Pipeline (Point 1/4)



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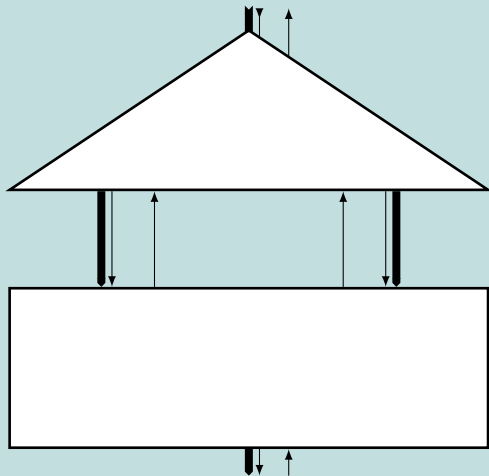


Control Buffer:  
Register diverts token when  
downstream suddenly stops

Cao et al. MEMOCODE 2015

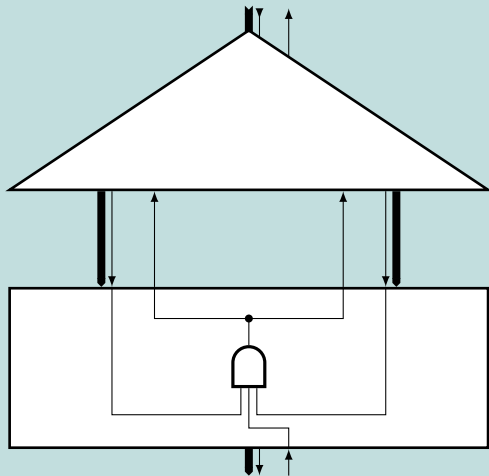
Inspired by Carloni's Latency Insensitive Design (e.g., MEMOCODE 2007)

# The Problem with Fork



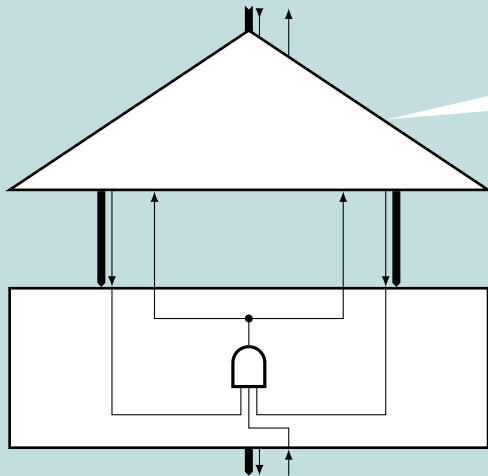
Combinational Block:  
inputs ready when  
both valid &  
output ready

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Combinational Block:  
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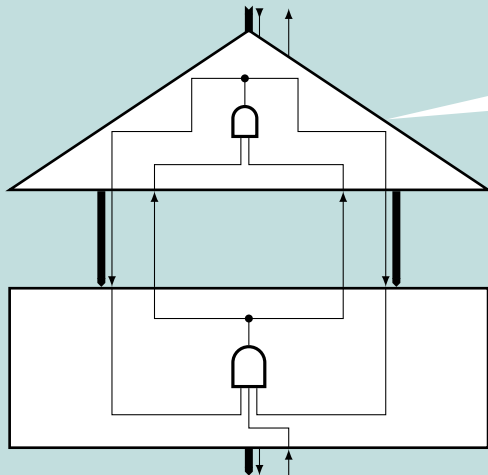
# The Problem with Fork



Fork:  
outputs valid only  
when all are ready

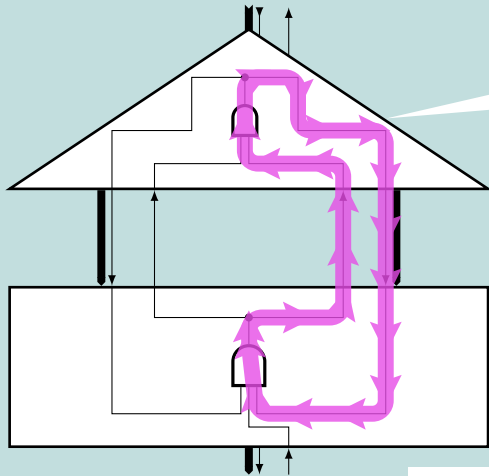


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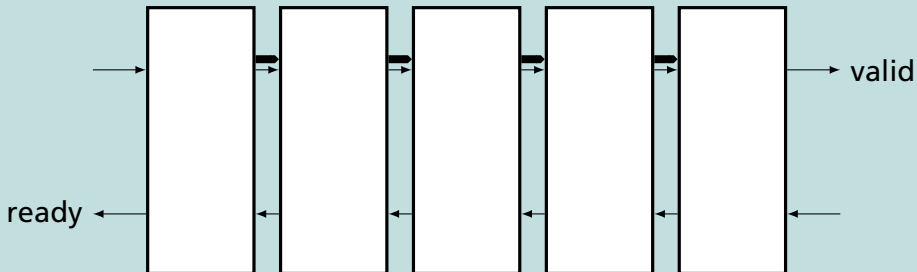
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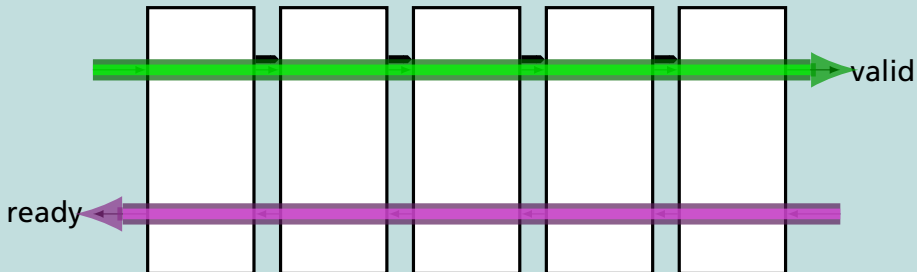
Fork:  
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Oops: Combinational Cycle  
This is *not* compositional

## The Solution to Combinational Loops (Point 2/4)

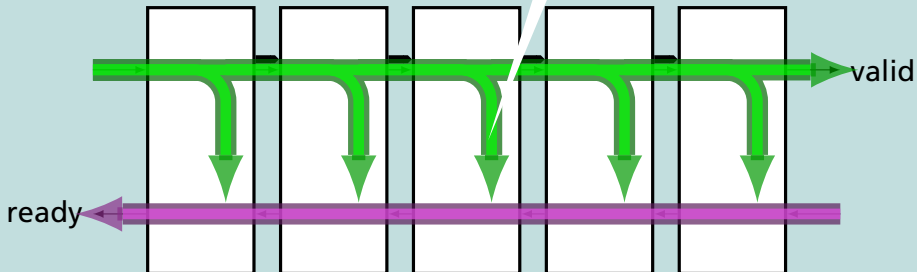


## The Solution to Combinational Loops (Point 2/4)



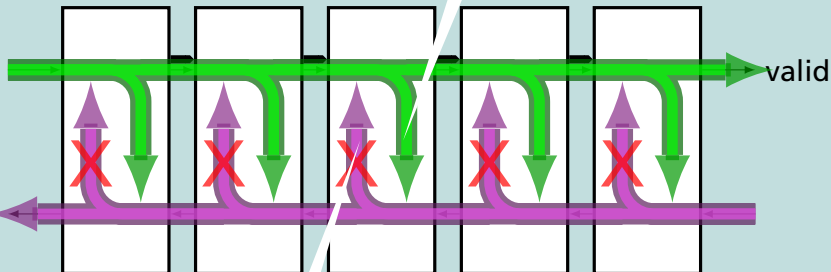
## The Solution to Combinational Loops (Point 2/4)

Allowed: Combinational paths from valid to ready



## The Solution to Combinational Loops (Point 2/4)

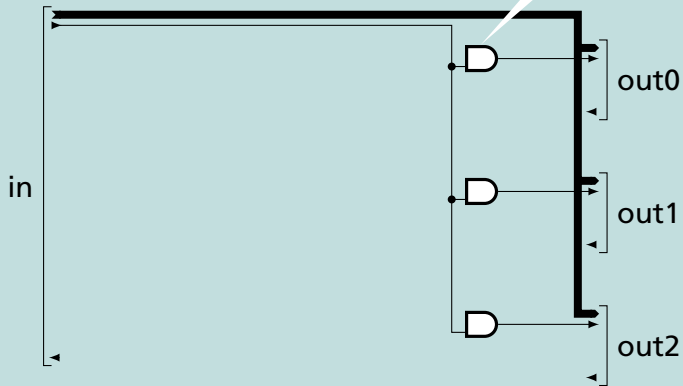
Allowed: Combinational paths from valid to ready



Prohibited: Combinational paths from ready to valid

## The Solution to Fork: A Little State (Point 3/4)

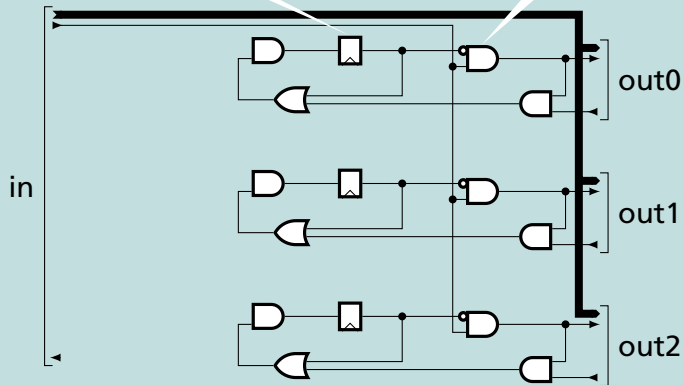
Valid out ignores ready of other outputs



## The Solution to Fork: A Little State (Point 3/4)

Flip-flop set after token sent suppresses duplicates

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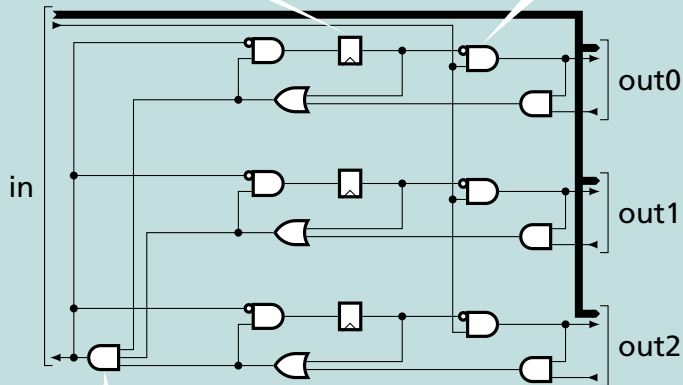




## The Solution to Fork: A Little State (Point 3/4)

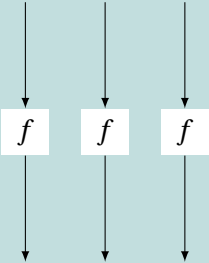
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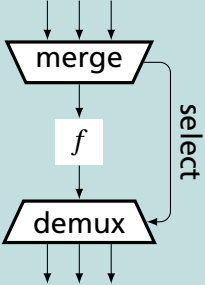


Input consumed once one token sent on every output

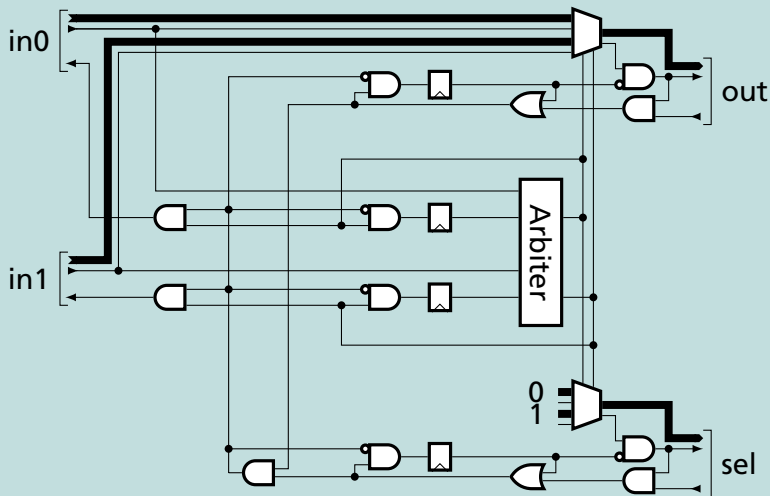
# Nondeterministic Merge (Point 4/4)



Share with merge/demux



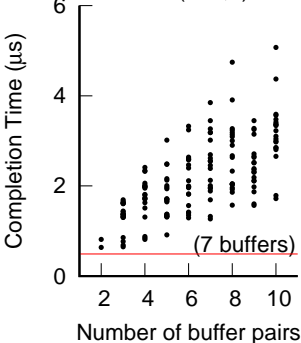
## Two-Way Nondeterministic Merge Block w/ Select



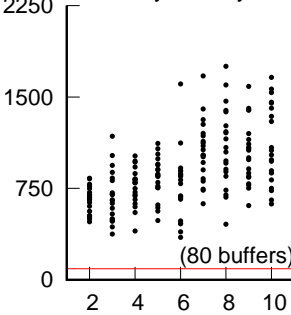
"Two-way fork with multiplexed output selected by an arbiter"

# Experiments: Random Buffer Placement

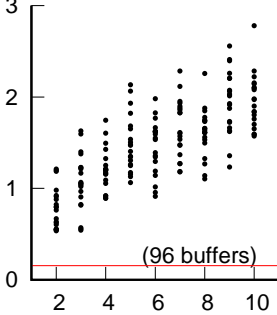
GCD(100,2)



21-way Conveyor

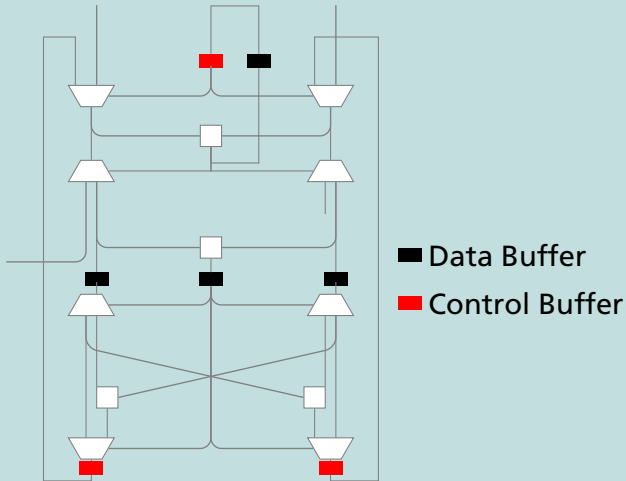


BSN



# Best Buffering for GCD (Manually Obtained)

Each loop has one of each buffer



# Summary

Compositional Dataflow Networks as an IR

Patient dataflow blocks with valid/ready handshaking

1. Break downstream, upstream paths w/ two buffer types
2. Avoid comb. cycles: prohibit ready-to-valid paths
3. Add one state bit per output so forks may “race ahead”
4. Tame nondeterministic merge with a select output

Random buffer placement experiments show it works