Hardware Acceleration for A Singularly Valuable Decomposition TYRION

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Overview

We intend to build a hardware accelerator for the singular value decomposition (SVD) and maybe the randomized SVD. Essentially, this will be a peripheral to compute basic matrix operations like matrix multiply, transpose, etc. Those basic steps can then be composed in hardware to compute subportions of a Jacobi SVD algorithm using the Kogbetliantz method, which is very parallelizable. This approach was implemented by Ma, Kaye, et al in 2006 [3]. We will also be consulting other supplementary sources to determine the final implementation [1, 2]. We will optimize the algorithm specifically for the SoCKit by appropriately splitting the workload between the onboard ARM processor and the FPGA.

Evaluation

Our evaluation will involve comparing the performance of our joint hardware-software implementation against a pure software implementation. This implementation will be either obtained or written and serve as the origination of our porting.

Project Requirements

Our project requires only the Cyclone SoCKit board. We will be utilizing the ARM processor as well as the FPGA to optimize the performance of the SVD algorithm.

Milestones

1. Implement an SVD algorithm in C
2. Define interface between onboard processor and FPGA
3. Implement an SVD algorithm split between the FPGA and ARM processor

References

[1] M. W. Berry, D. Mezher, B. Philippe, and A. Sameh. Parallel algorithms for the singular value decomposition. *Statistics Textbooks and Monographs*, 184:117, 2006.

[2] N. Halko, P.-G. Martinsson, and J. A. Tropp. Finding structure with randomness: Probabilistic algorithms for constructing approximate matrix decompositions. *SIAM review*, 53(2):217–288, 2011.

[3] W. Ma, M. Kaye, D. Luke, and R. Doraiswami. An fpga-based singular value decomposition processor. In *Electrical and Computer Engineering, 2006. CCECE '06. Canadian Conference on*, pages 1047–1050, May 2006.