CSEE W3827

Fundamentals of Computer Systems

Homework Assignment 2

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Columbia University

Due June 18th, 2015 at 5:30 PM

Write your name **and UNI** on your solutions

Show your work for each problem; we are more interested in how you get the answer than whether you get the right answer.

You may use Logisim to draw your circuits. We also suggest you use Logisim to verify them.

1. (20 pts.) A sequential circuit with two D flip-flops S_0 and S_1, two inputs X and Y, and one output Z behaves according to these equations:

$$S_0' = \overline{X}Y + XS_0 \quad S_1' = XS_1 + \overline{X}S_0 \quad Z = XS_0$$

(a) Draw the corresponding circuit. Label each of the signals mentioned above.

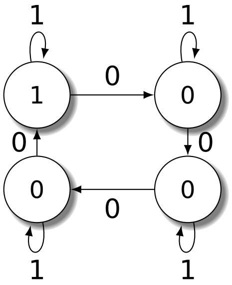
(b) Derive the state table (next state and output as a function of present state and input).

(c) Draw the corresponding bubble-and-arc diagram.

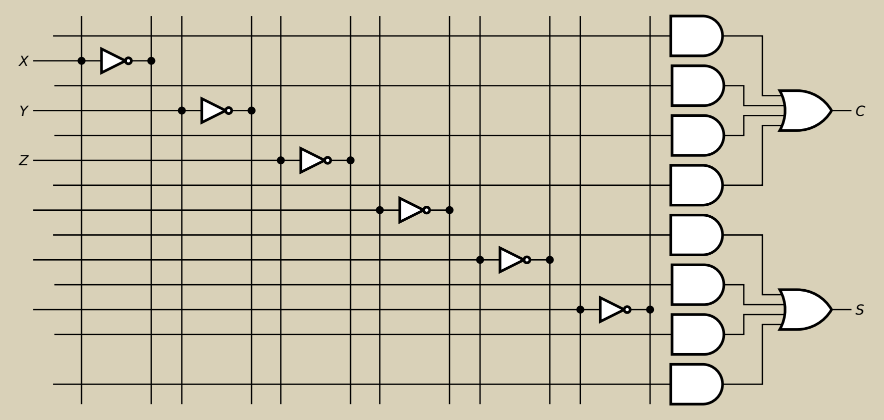
2. (20 pts.) Determine the logic for a synchronous 4-bit counter that counts 0,1,. . . ,9,10,11,0,1,. . . in binary. It should have four outputs Q_1, Q_2, Q_4, Q_8, (the subscripts indicate the value of each bit) each driven directly by a flip-flop.

   Write Boolean expressions of the form $D_i = Q_i \oplus (\cdots)$ for each flip-flop's input. ($\oplus$ is XOR) You do not have to submit a schematic for this problem.

3. (20 pts.) Using just four flip-flops and four two-input muxes, draw a circuit for the following Moore state machine with a single input and single output. Use a one-hot encoding. Each state is labeled with the value of the output.



4. (20 pts.) Show how to implement a full-carry adder using the PLA drawn below.
Hint: write the expressions for *S* and *C* in sum-of-products form then draw crosses to indicate connections on the AND plane.



5. (20 pts.) The circuit below is called a linear-feedback shift register. Draw a bubble-and-arc diagram representing its behavior. Start from both the state $X = 0$, $Y = 0$, $Z = 1$ and the all-zeros state.