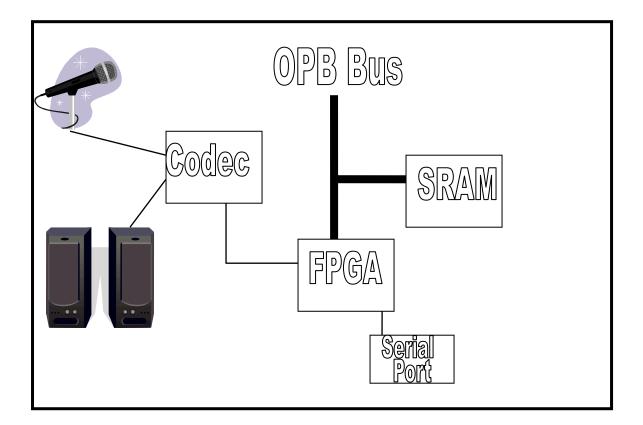
# Digital Voice Recorder CSEE4840 – Embeded System Design

Stephanie Maryon (sem2134) Adegoke Adediran (aoa2001)

## Introduction:

The goal of our project is to design a digital voice recorder. Our voice recorder will give the user the option to either record their voice or to have it directly come out of the speaker. Once we can record to memory we will implement a simple file system that will allow us to record and store multiple voice clips. If time permits we will enable the file system to play back individual clips. Our design includes use of the AKM AK4565, the Toshiba TC55V16256J 256k X 16 SRAM, the Serial Port, the Xilinx Spartan-IIE 1.8V FPGA of course, and the OPB Bus in order to coordinate our system.



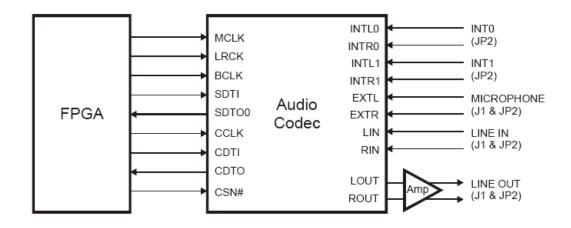
### **Design Components:**

#### The AKM AK4565:

The AKM AK4565 is an audio codec which enables us to hook up a microphone and speakers to our system. We are using the codec to either accept an analog signal

from the microphone, convert it to a digital signal and send the bits to the FPGA, or to receive a digital stream of bits from the FPGA, convert the stream to an analog signal and output the signal through speakers. We are going to set the codec to have an 8KHz sampling rate into to achieve the maximum recording time.

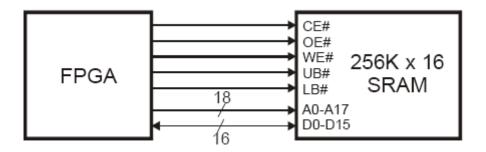
The codec connects to the FPGA as shown. We will be using the Extr inputs to connect the microphone and the Out outputs to connect the speakers. In our implementation we will only record one of the channels from the microphone to the SRAM which will double our recording time.



#### The Toshiba TC55V16256J 256k X 16 SRAM:

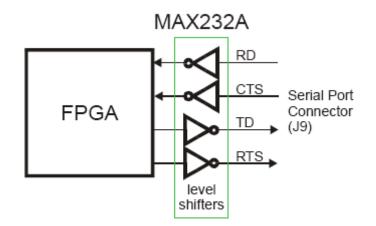
We will be recording the samples from the microphone into the on-board SRAM. The SRAM is organized as a 262,144, 16-bit array. We chose to make each sample we receive from the codec 16 bits long. Therefore our memory will be able to hold 262,144 samples. This gives us a maximum recording time of about 65.5sec.

2(only reading one channel) \*262,144/8k = 65.5sec.



#### The Serial Port:

The serial port is going to be used for control inputs to our system. This will enable the user to be able to speak directly from the microphone into the speakers, or to record, stop, or play back their voice. The play back control will be simple and just play back all of the memory.



#### The FPGA and OPB Bus:

The FPGA will be used to make registers, FSM, and any other hardware pieces that we might need to implement our system. FSM will be used in order to coordinate the codec, the SRAM, and the serial port when using the OPB Bus.