Compiling Esterel into Better Circuits

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Esterel

- Characters effecting circuitry translation
  - High level control constructs
    - More complex, more challenges
    - Better understanding of program behavior
      - Enable aggressive optimization
  - Explicit and implicit pause statement
    - Implicit state machine

3 Stages of Circuit Translation

- 1. State assignment
  - Base on Program Dependence Graph (PDG) [9,2]
- 2. Hardware synthesis
  - Straight forward when coding has been chosen
- 3. Circuit optimization
  - 1) sequential optimization
    - State encoding
  - 2) combinational optimization
    - SIS

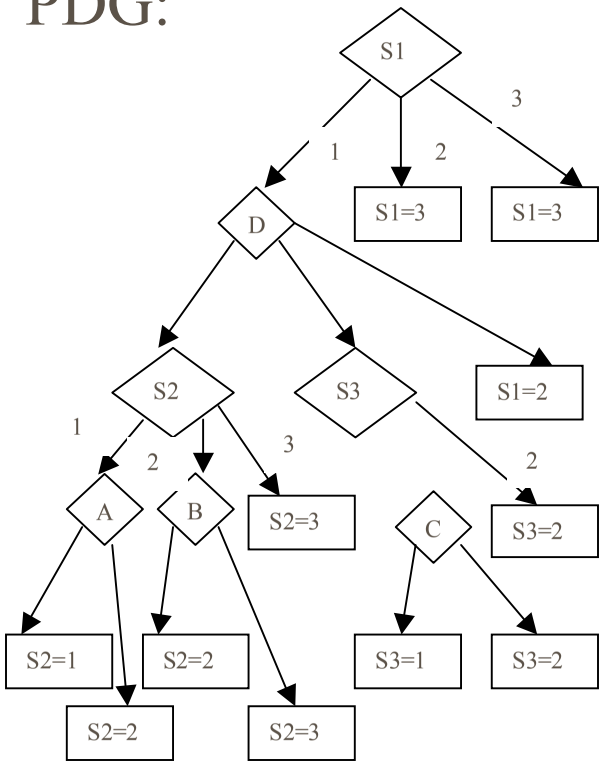
An Example of PDG

- An example program:

- abort
- [
- await A; await B
  ||
  await C;
  ]
  when D;

pause;

PDG:



State Encoding

- Heuristic Search
  - Find a solution with fewest latches under the requirement
  - Or, exhaust the search space
- Search Space
  - 1. Berry's one-hot encoding [1]
  - 2. Edwards's group-hot-by-level encoding [2]
  - 3. Variant

Classic State Assignment

- Based on Finite State Machine
- Reduce reachable state by minimizing the incomplete specified machines

NOVA: Two-level logic optimization

- Basic concept: State code adjacency
- Constraint satisfaction to graph-embedding problem
- Best strategy: iohybrid_code
  - ihybrid_code
    - 1 Partition input constrains to SIC, RIC
    - 2 Encode with minimum length under SIC
    - 3 Increase embedding cube to satisfy RIC within encoding space
  - ihybrid_code + output constrains

MUSTANG: Multilevel logic optimization

- Basic concept: State code adjacency
- Aim: maximize the size and number of common cubes
- Tool: Attraction Graph with weighted edges

Berry's Method of Translation

- First outlined in 1992 [1]
- Hardware synthesis
  - Sub-circuit for each statement
  - Registers only for pause statement
- Encoding leaf states by one-hot coding
  - Encoding/decoding circuits are trivial
  - Reachable state space redundant

Sentovich, Toma and Berry: the technique latches reducing

- Steps:
  - 1. Compute reachable state set using BDDs
  - 2. Remove sequential redundancies and re-synthesizing the circuit

Edwards's Advanced Method

- 1. CFG: New structural translation
  - More efficient at removing redundant circuits than removing by analyzing the circuit
- 2. Better state encoding
  - High level encoding – greater flexibility and larger encoding space
- 3. Don't care information
  - Helpful to logic synthesis

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